

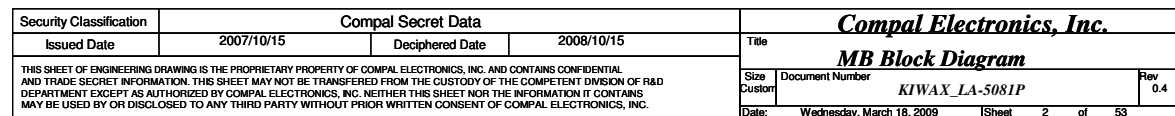
KIWA7/A8

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic

REV: 0 . 4

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DDR3 Voltage Rails

<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICKL_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	V	X	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

VGA and DDR2 Voltage Rails (N10M)

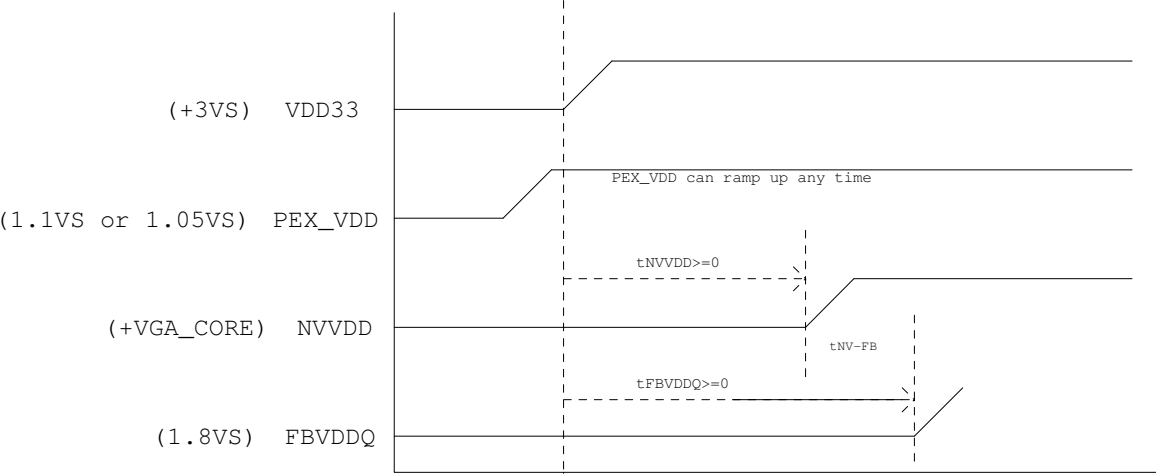
power plane	State			
				+3VS +VGA_CORE +1.1VS (for 55nm) +1.05VS (for 40nm) +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		N10M-GE1-S	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SEQUENCE

The ramp time for any rail must be more than 40us



Width=4 mil ,
Spacing: 15mil
(55Ohm)

Layout note: Z0=55 ohm
0.5" max for GTLREF.

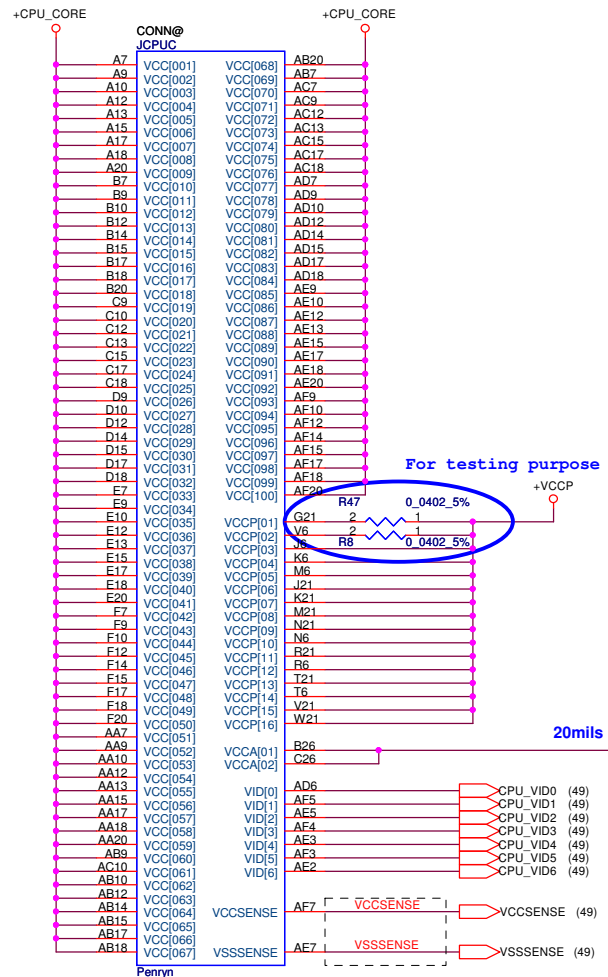
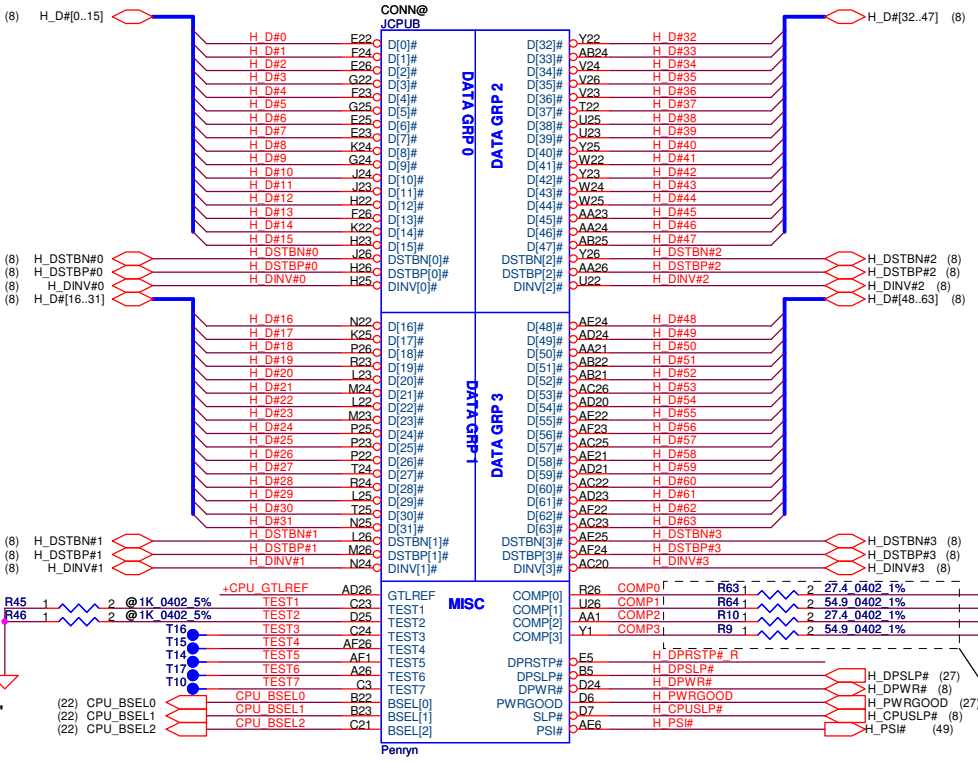
Close to CPU pin AD26
within 500mils.

Trace Close CPU < 0.5"

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

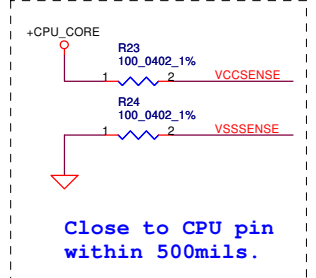
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

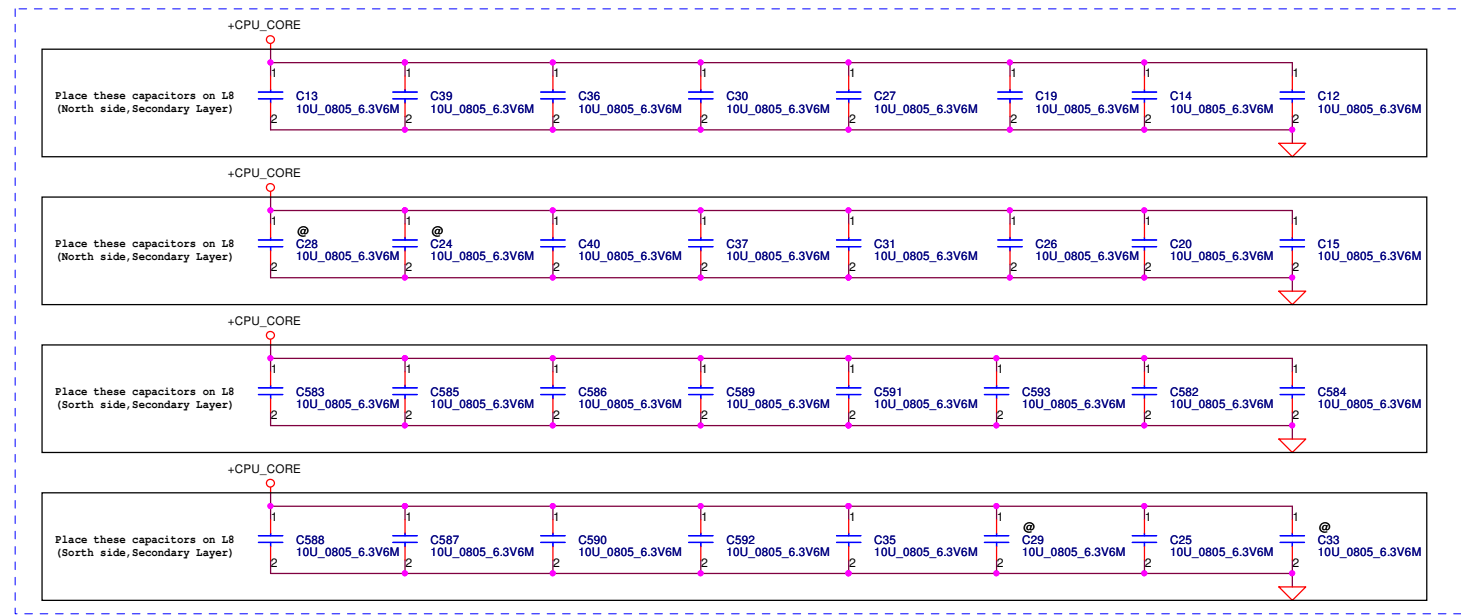


Length match within 25 mils.
The trace width/space/other is
16/7/25.

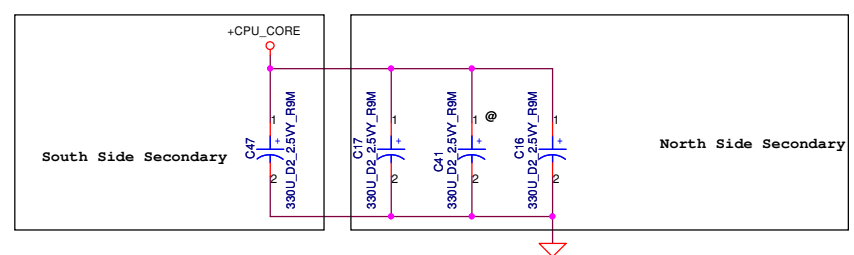
Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



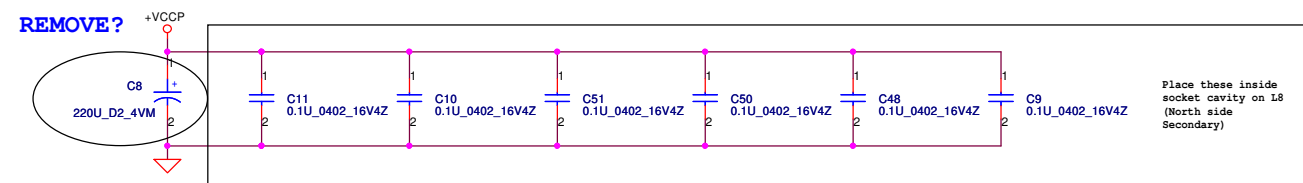
CONN@ JCPUD		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
	VSS[082]	AF25



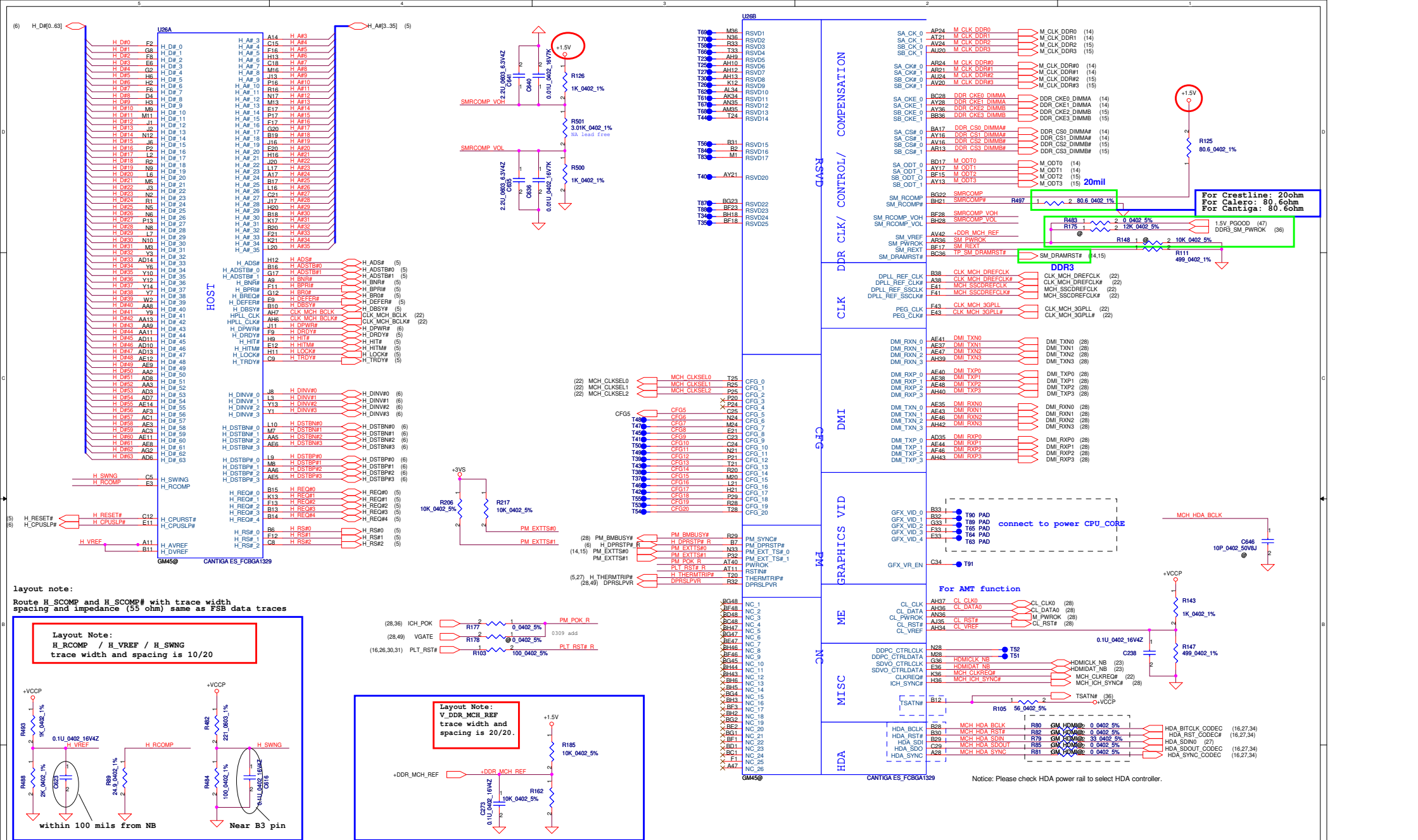
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

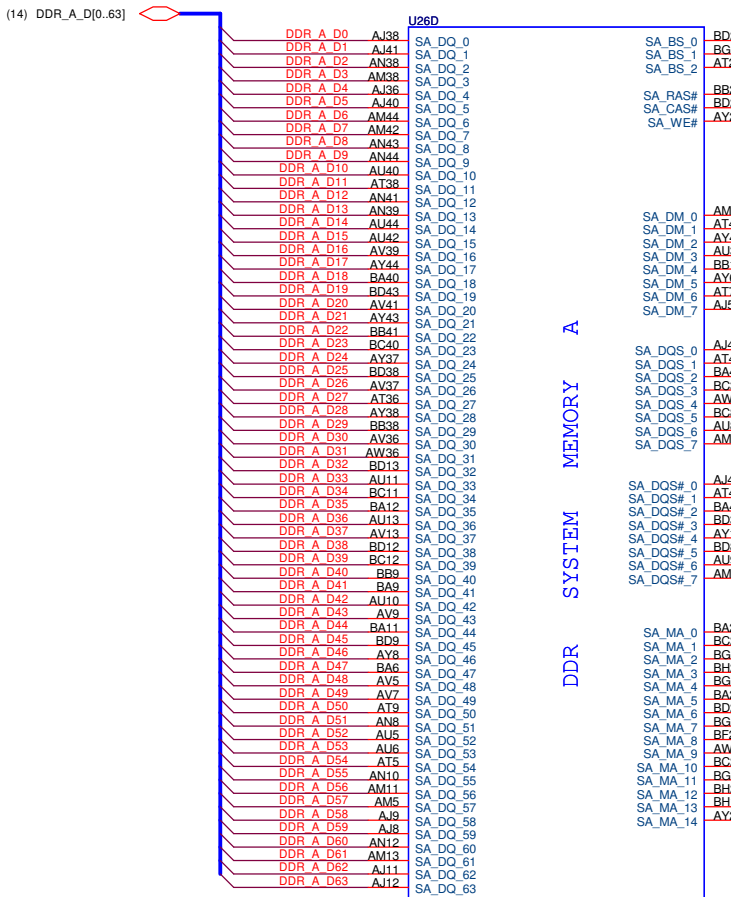


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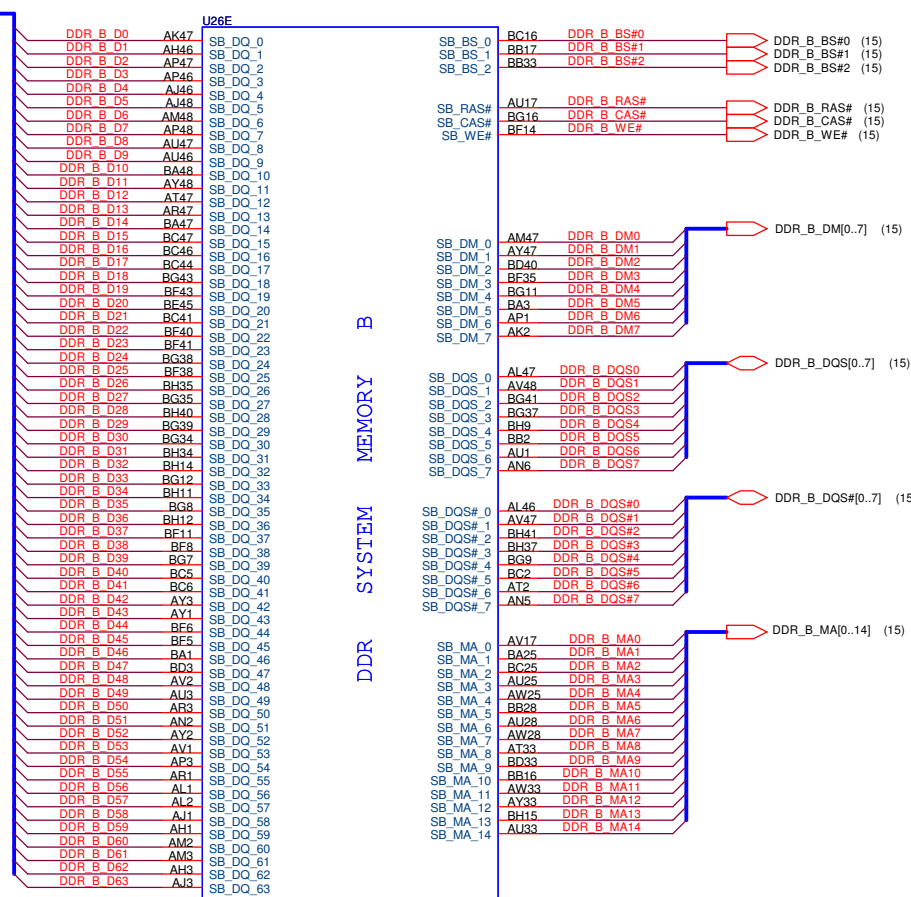
(14) DDR_A_D[0..63]



GM45@

CANTIGA ES_FCBGA1329

(15) DDR_B_D[0..63]

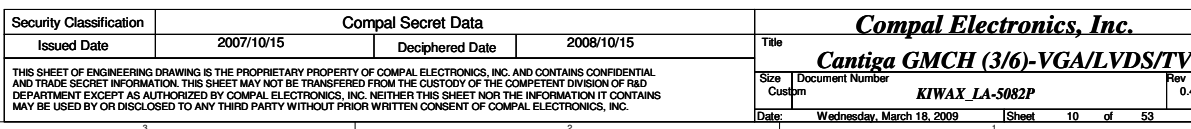


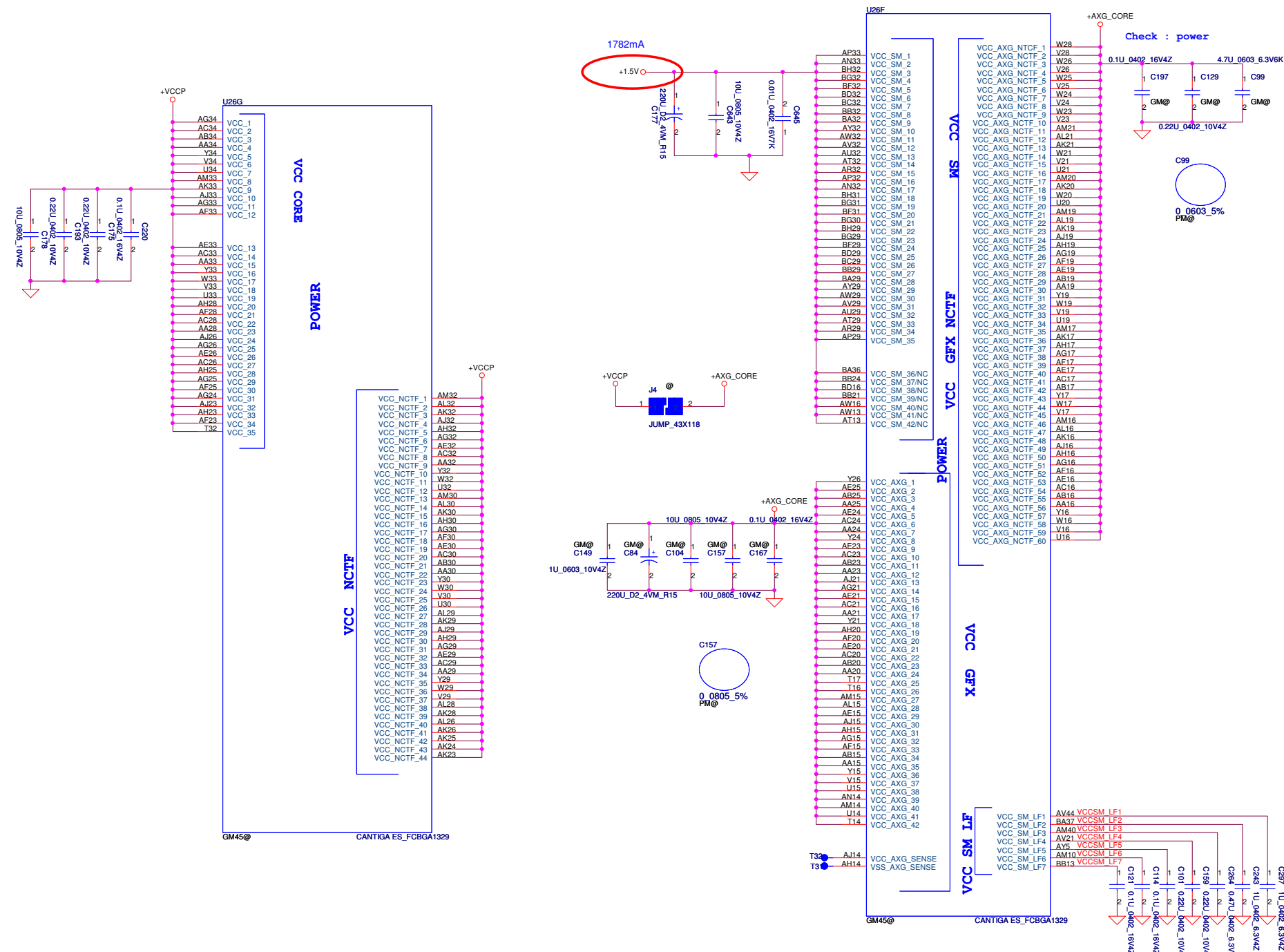
GM45@

CANTIGA ES_FCBGA1329

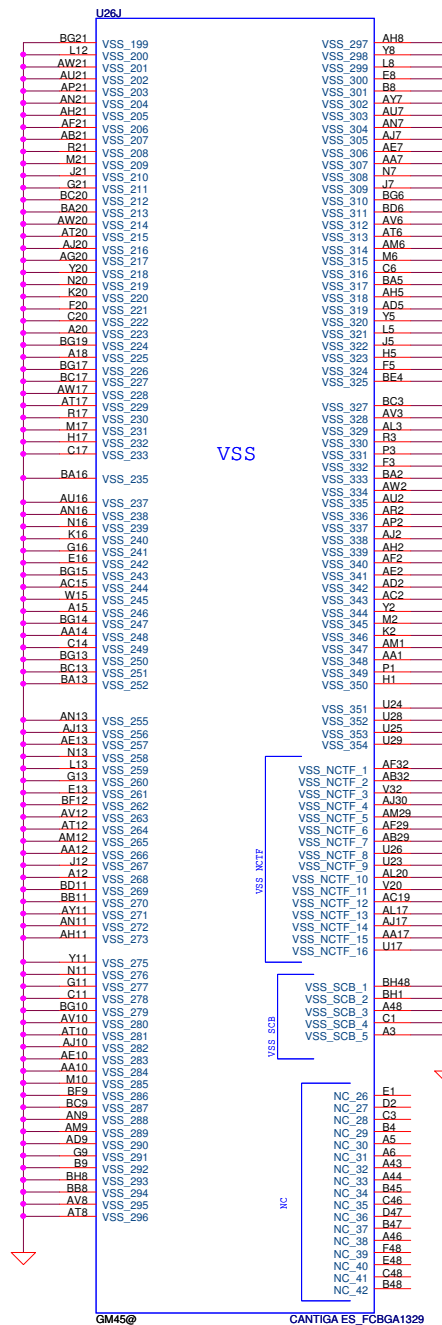
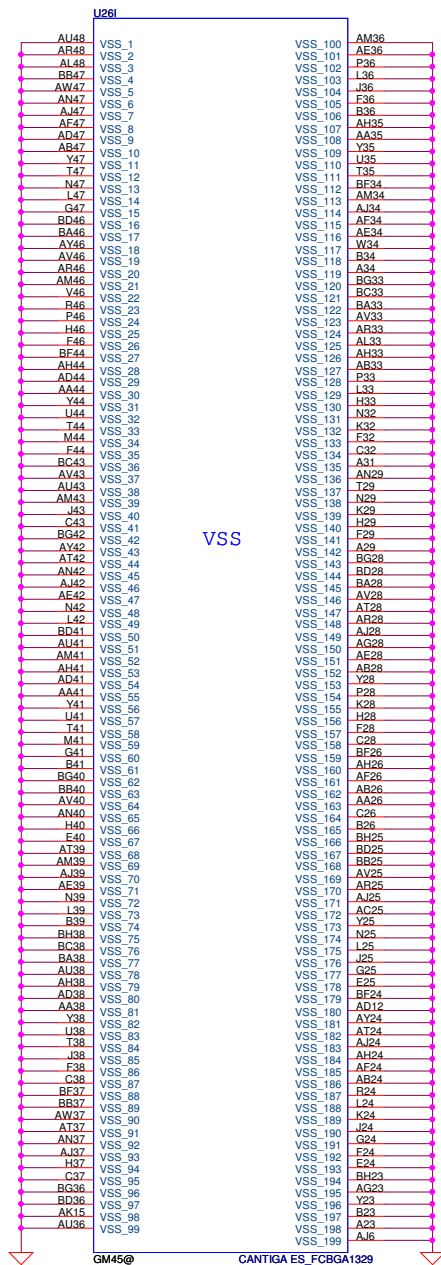
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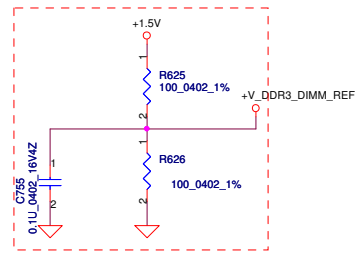




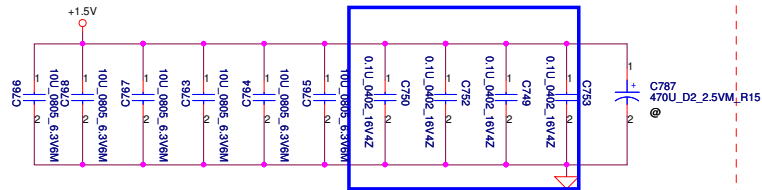
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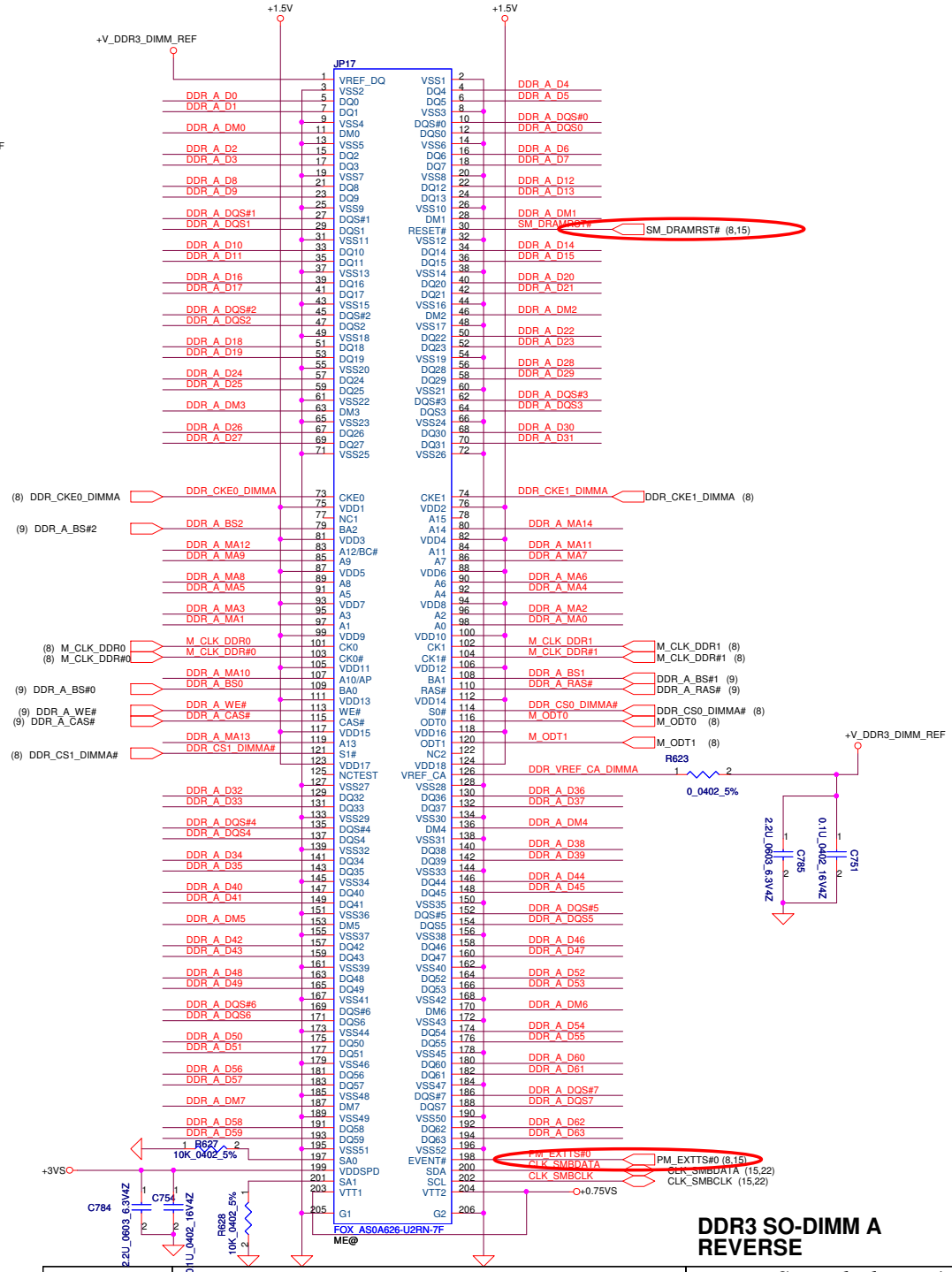
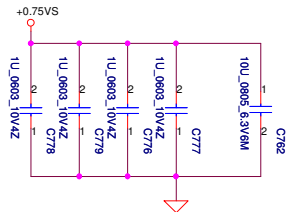
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Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

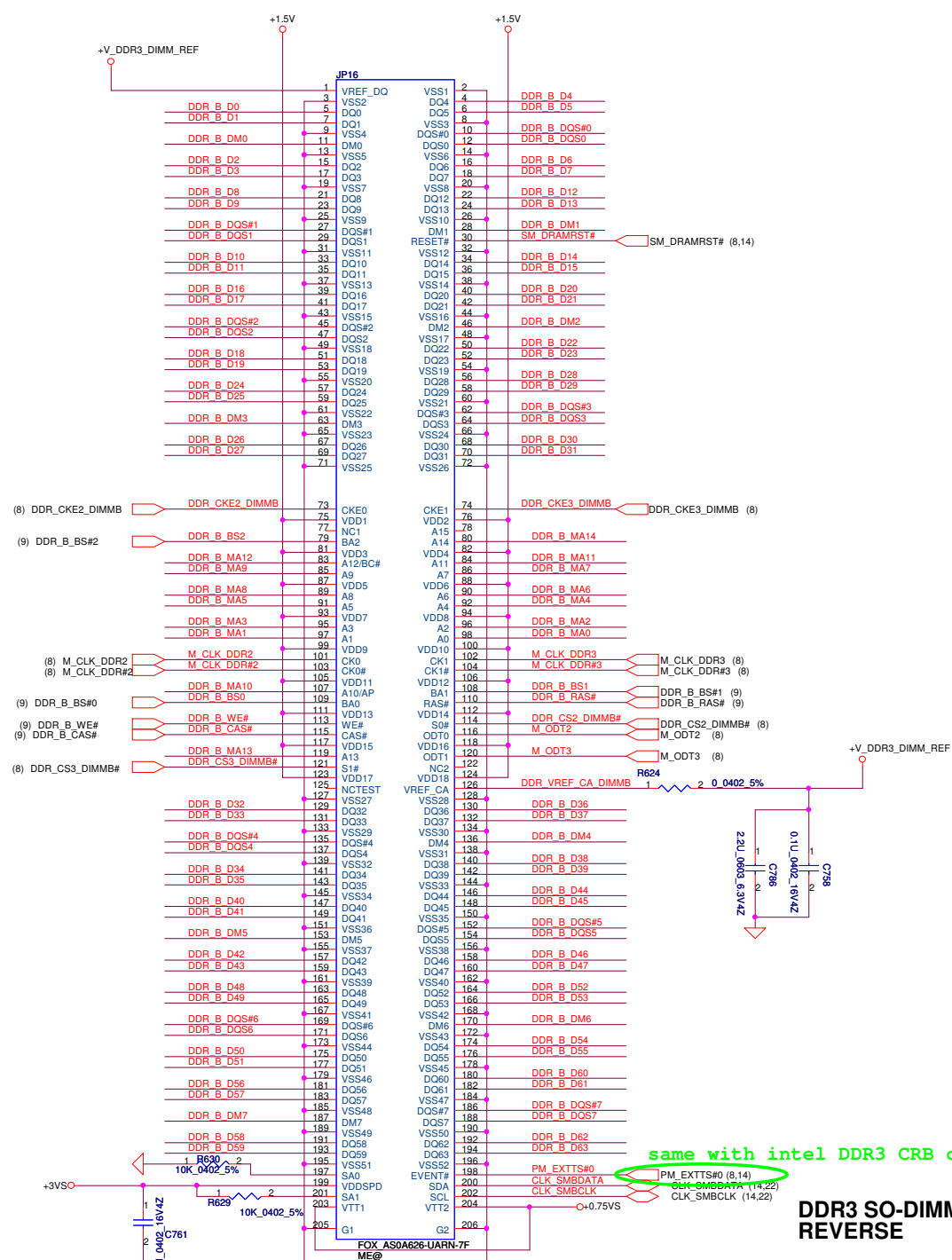
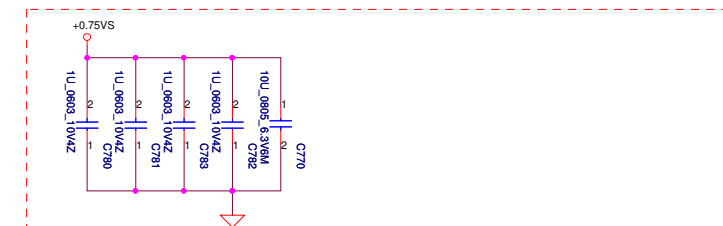
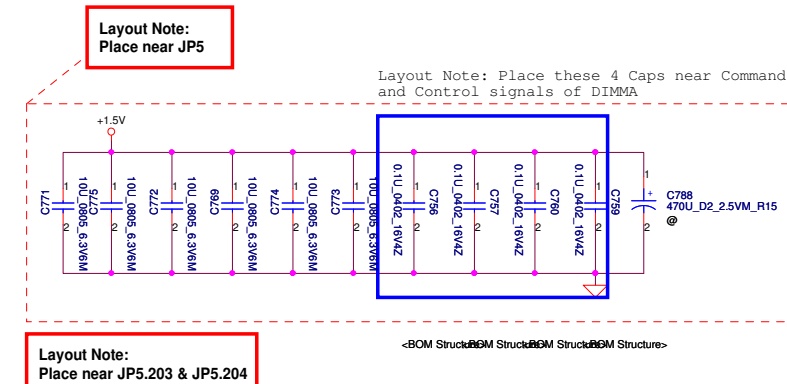
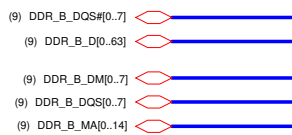


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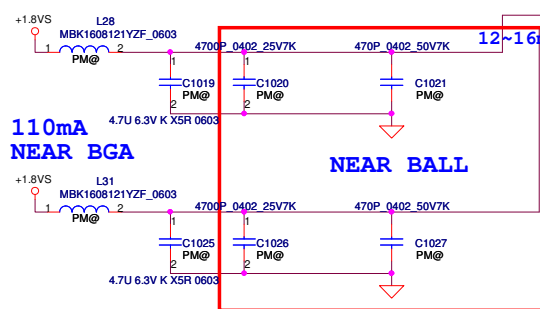
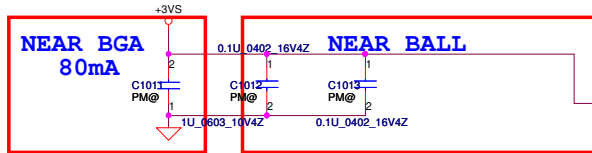
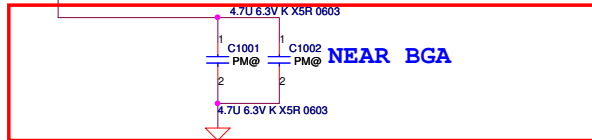
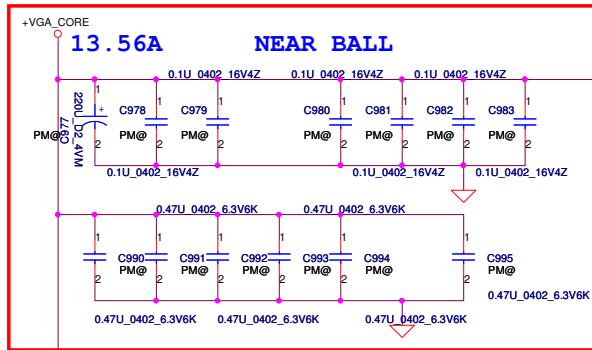
	<i>Compal Electronics, Inc.</i>
Title	<i>DDRIII-SODIMM SLOT1</i>

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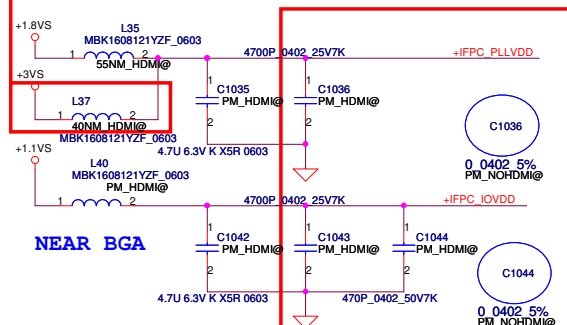


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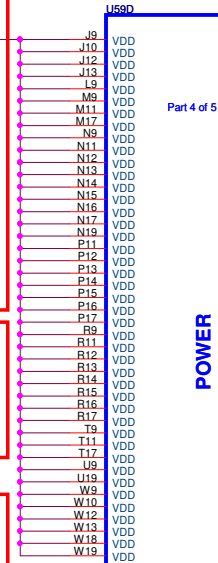
FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS



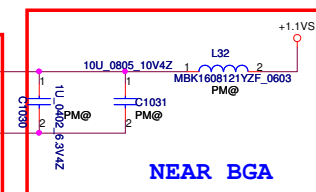
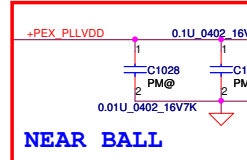
IFPC_PLLVDD: please add option to support both 1.8V (for G9X) and 3.3V(for GT21X)



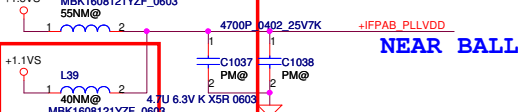
NEAR BALL



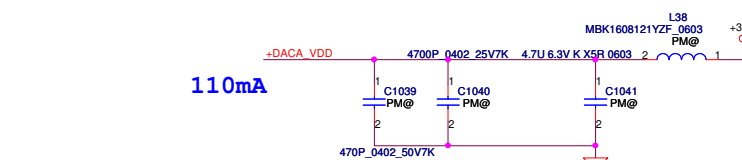
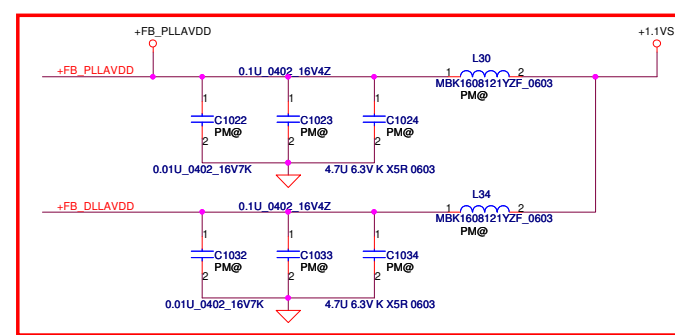
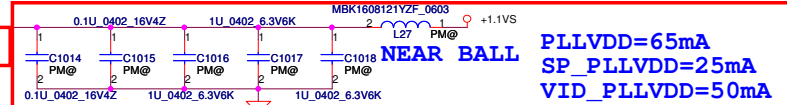
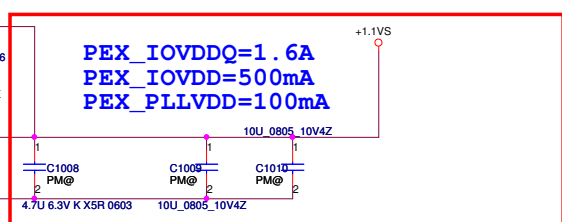
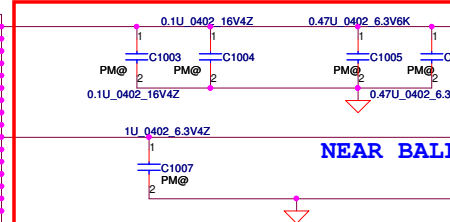
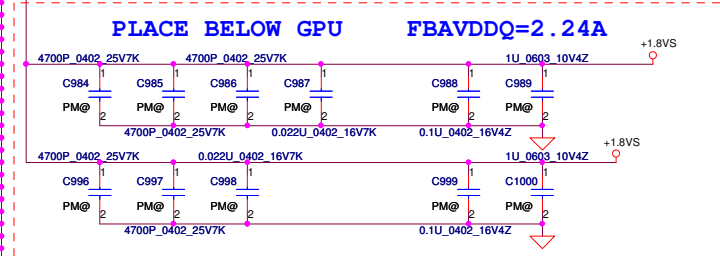
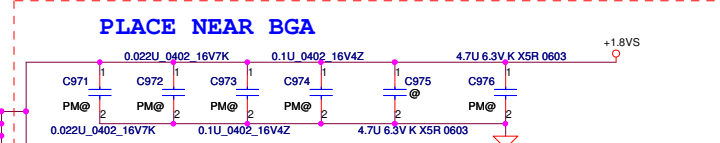
12~16mii



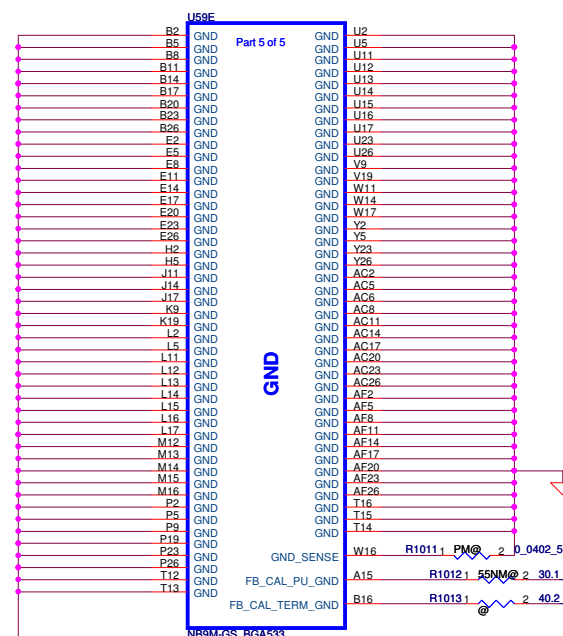
260mA NEAR BGA



IFPAB_PLLVDD: please add option to support both 1.8V(for G9X) and 1.05V(for GT21X)



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				Document Number	KIWA5/6 LA-5081P
				Rev	0.4
				Date	Wednesday, March 18, 2009
				Sheet	18 of 53



Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

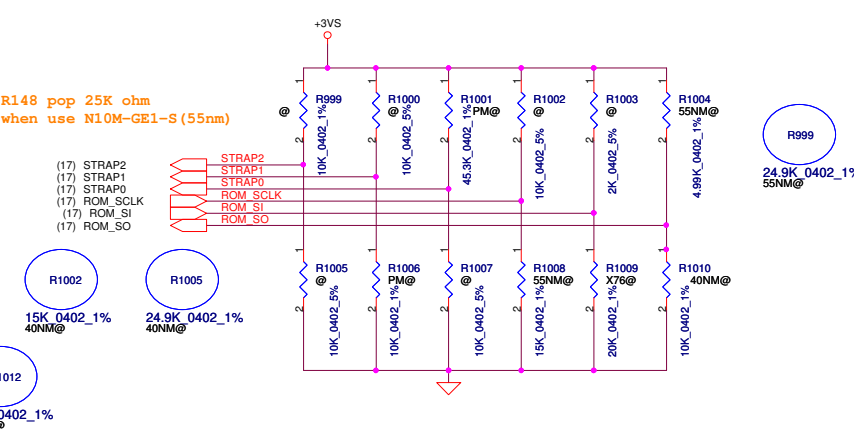
To update for NV PUN-03304-001_V06 (2008/4/01)



A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available

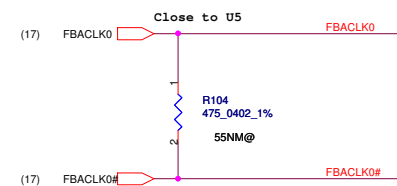
R148 pop 25K ohm
 when use N10M-GE1-S (55nm)

- (17) STRAP2
- (17) STRAP1
- (17) STRAP0
- (17) ROM_SCLK
- (17) ROM_SI
- (17) ROM_SO



GB1 Family GPU Strap Options

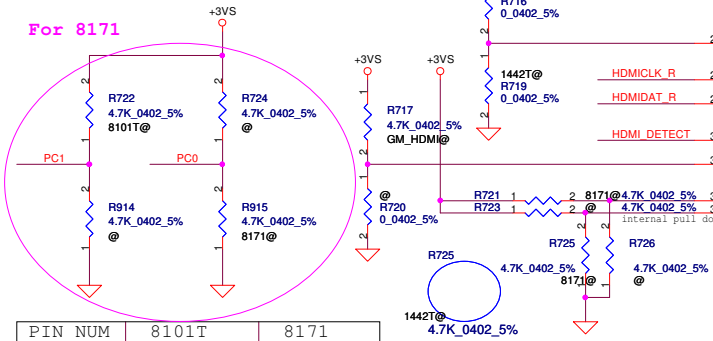
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 5K	PD 10K PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K PU 45K
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 10K PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 10K PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K PU 45K



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							VRAM DDRA					
							Size	Document Number	Rev			
							Custom	KIWA5/6 LA-5081P	0.4			
Date:							Wednesday, March 18, 2009		Sheet		20 of 53	

10/30 update PS8171 co-lay circuit

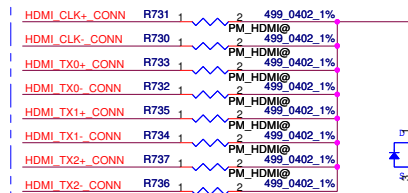
For 8171



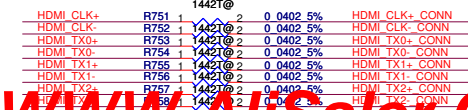
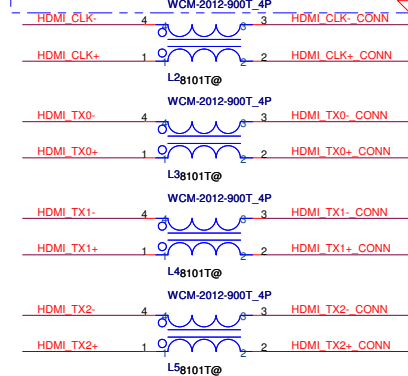
PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PTO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	ASQ1
PIN12	GND	APD
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DCCBUF_EN	DCCBUF
PIN35	CFG	PRE

```
For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD
```

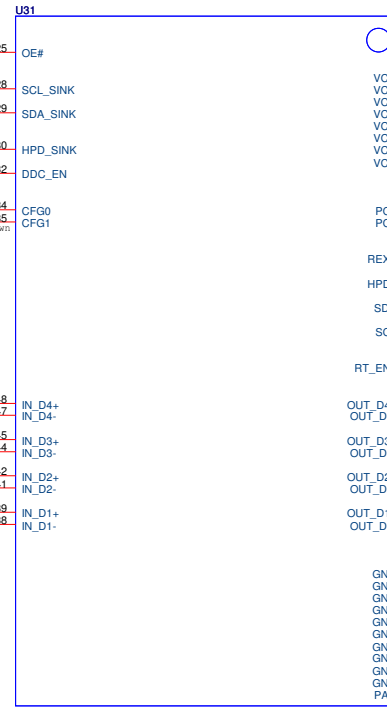
TMDS pull down (500ohm) resistors for ATI M92-S2 XT



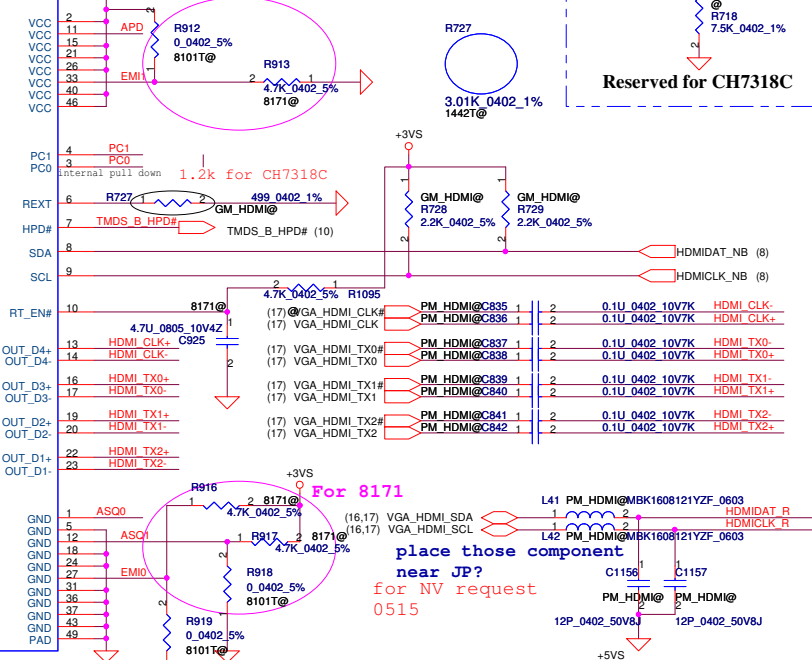
NEAR CONNECTOR



P/N: SA00002D700 (8101T)
P/N: SA00001U920 (CH7318C)



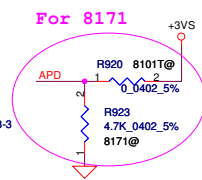
For 8171



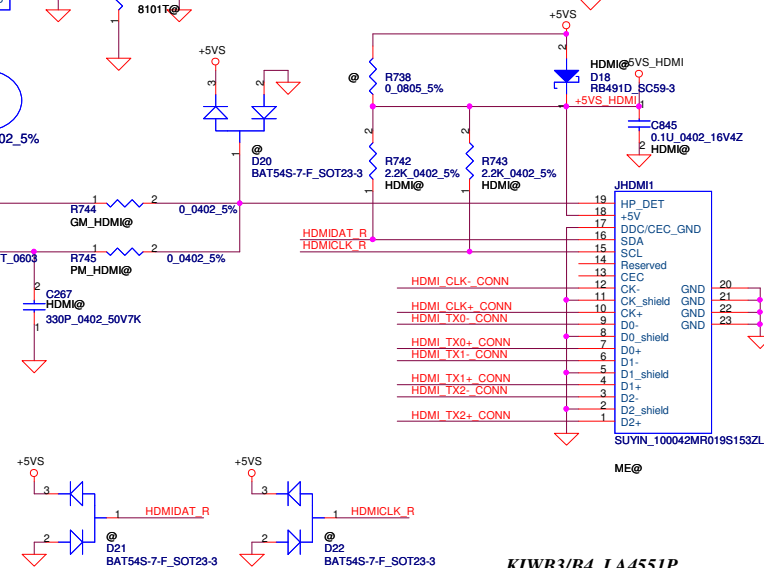
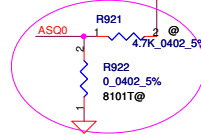
```

place those component
near JP?
for NV request
0515

```



For 8171

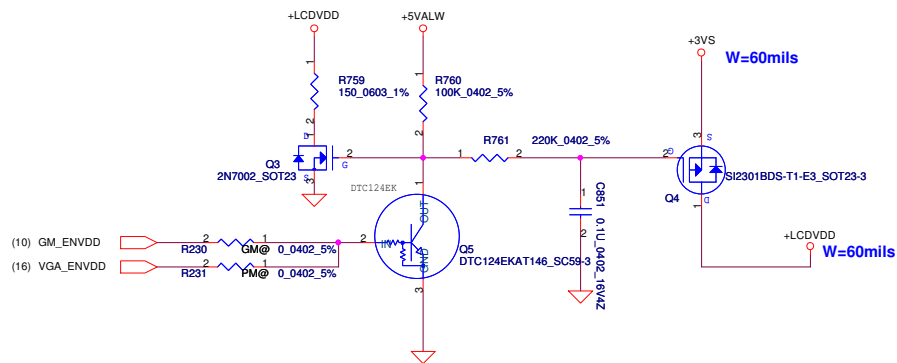


KIWB3/B4_LA4551P

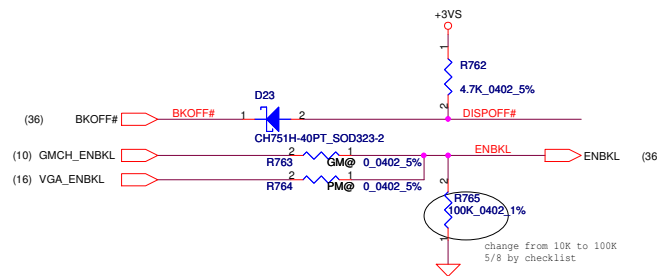
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter_PS8101T	
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				Custom		
				Date:	Wednesday, March 18, 2009	Rev 0
				Sheet	23 of 53	

HDMI TX2: R757 1 1442782.2 0.00 2.5% HDMI TX2+: CONN
 HDMI TX2: R758 1 1442782.2 0.00 2.5% HDMI TX2+: CONN
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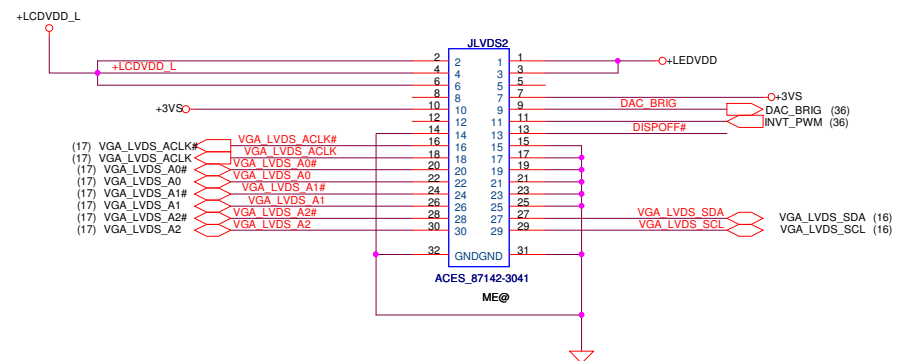
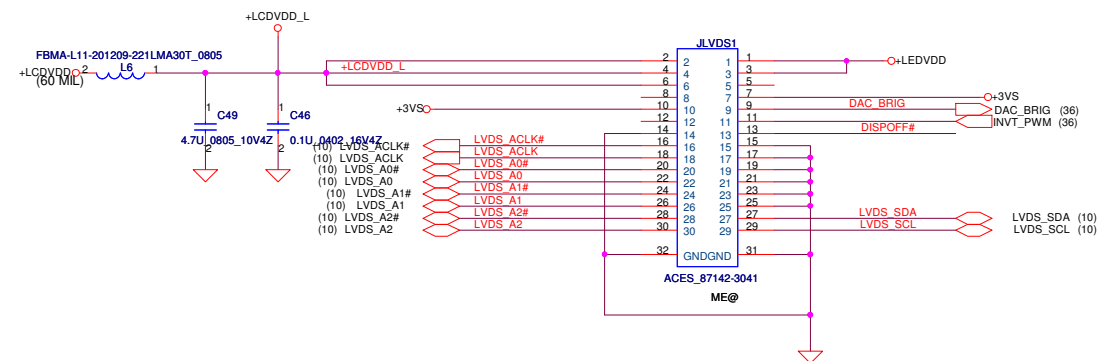
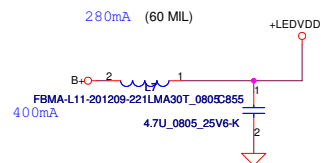
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.
FOR UMA



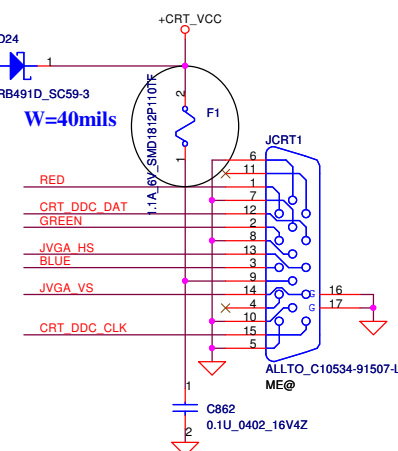
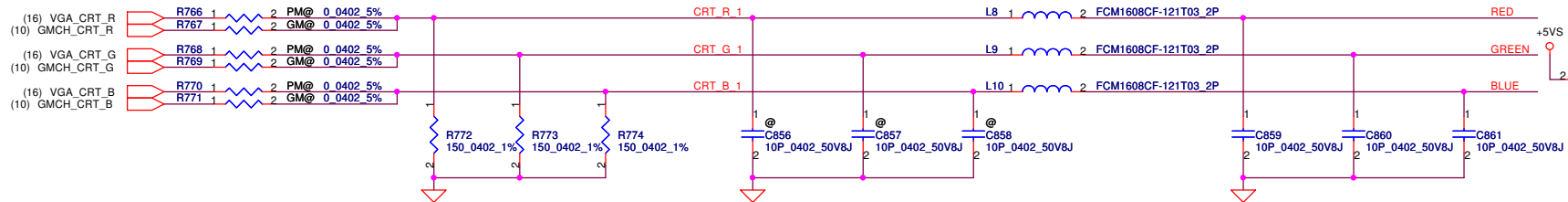
LCD/PANEL BD. Conn.
FOR DIS



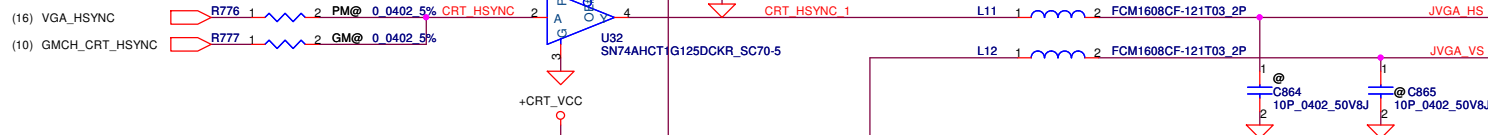
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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				KIWA5/6 LA-5081P	
				Date: Wednesday, March 18, 2009	Rev 0.4
				Sheet 24 of 53	

CRT Connector

CLOSE TO CONN



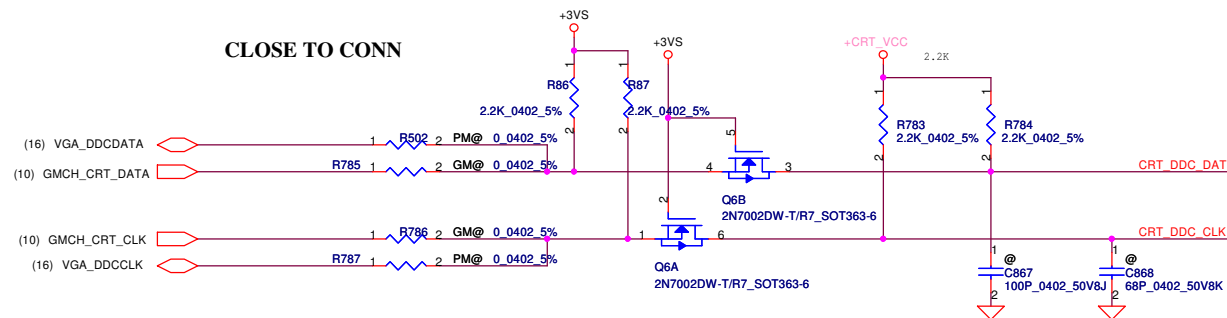
CLOSE TO CONN



CLOSE TO CONN



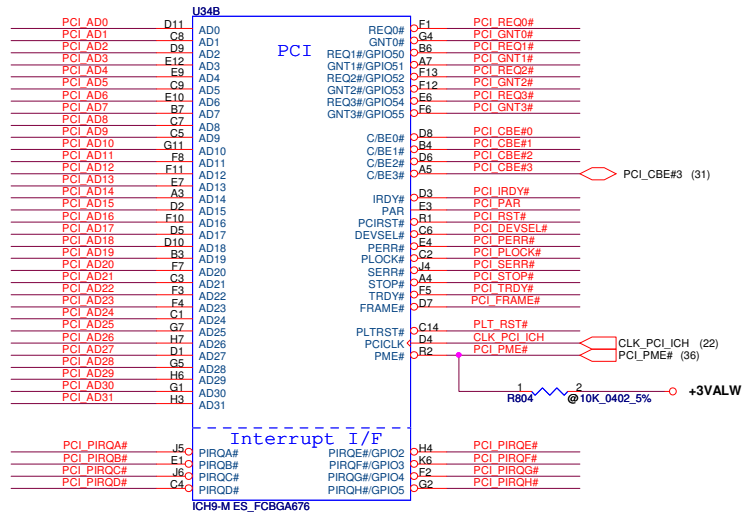
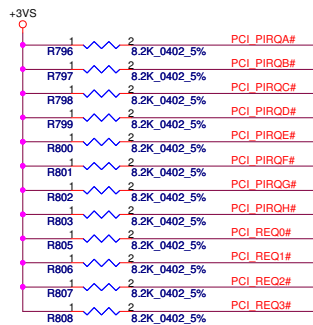
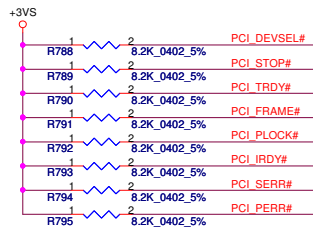
CLOSE TO CONN



PIN ASSIGMENT

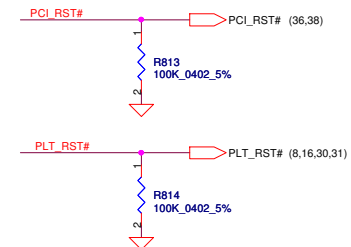
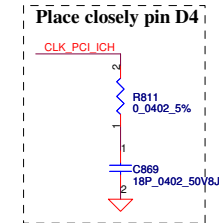
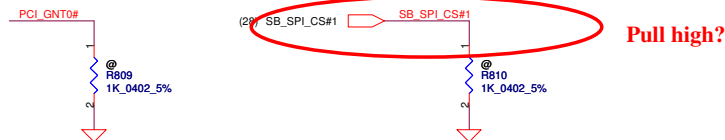
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

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Size	Custom	Document Number	KIWA5/6 LA-5081P	Rev	0.4
Date	Wednesday, March 18, 2009	Sheet	25	of	53



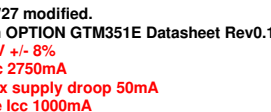
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



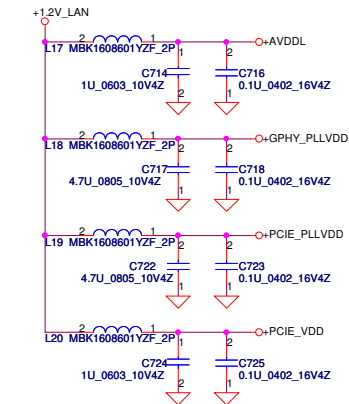
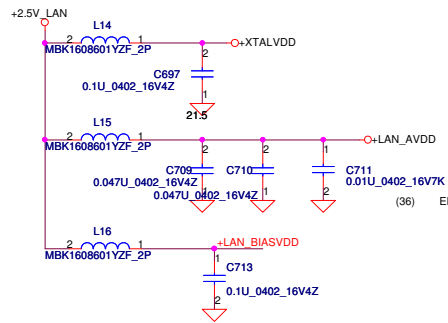


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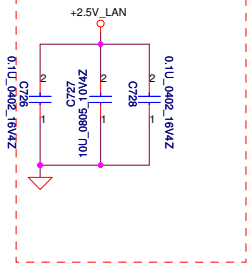


Security Classification		Compal Secret Data		Compal Electronics, Inc.							
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						Size	Document Number				Rev 0.4
							KIWX_LA-5082P				
						Date:	Wednesday, March 18, 2009		Sheet	30	of

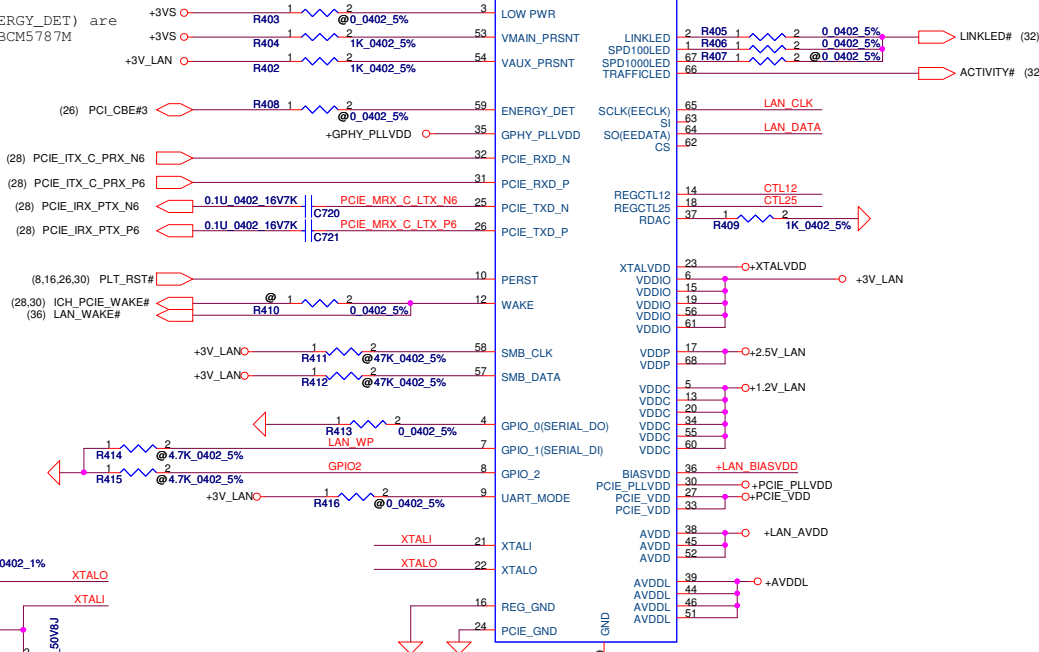
Layout Notice : Filter place as close chip as possible.



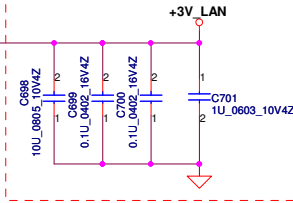
Layout Notice : Place as close chip as possible.



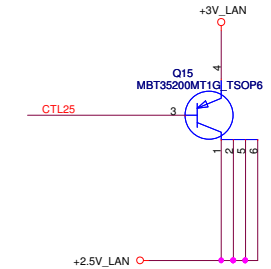
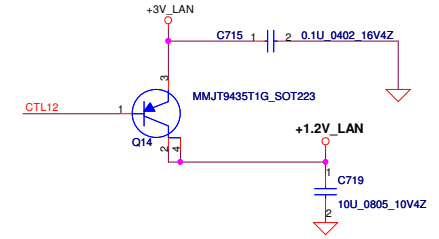
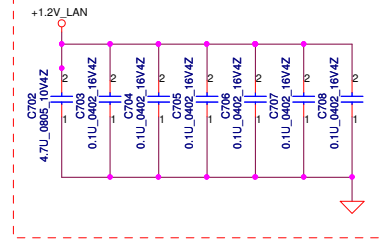
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Layout Notice : Place as close chip as possible.

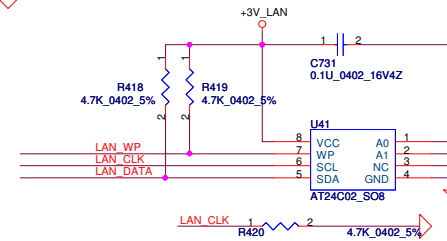


Layout Notice : 1.2V filter. Place as close chip as possible.



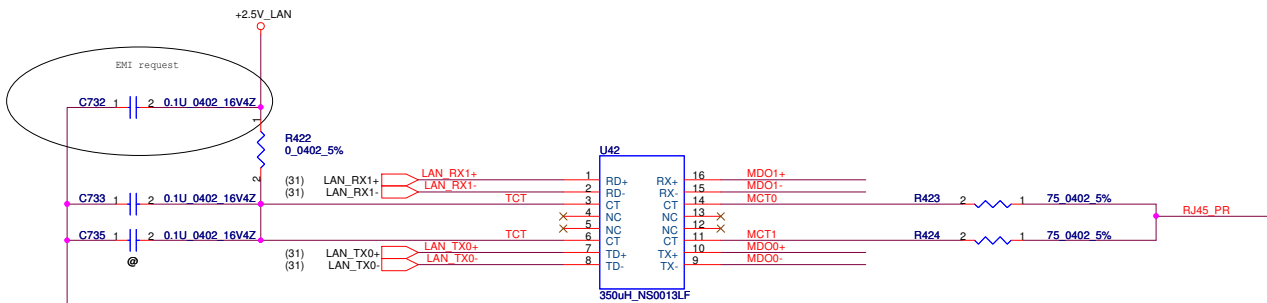
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

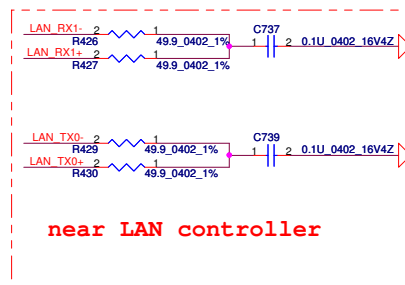


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2007/10/15				BCM5787MKML			
Deciphered Date				2008/10/15				KIWA5/6 LA-5081P			
Title				Wednesday, March 18, 2009				Sheet 31 of 53			
Size				Document Number				Rev 0.4			
Date				Wednesday, March 18, 2009				Sheet 31 of 53			

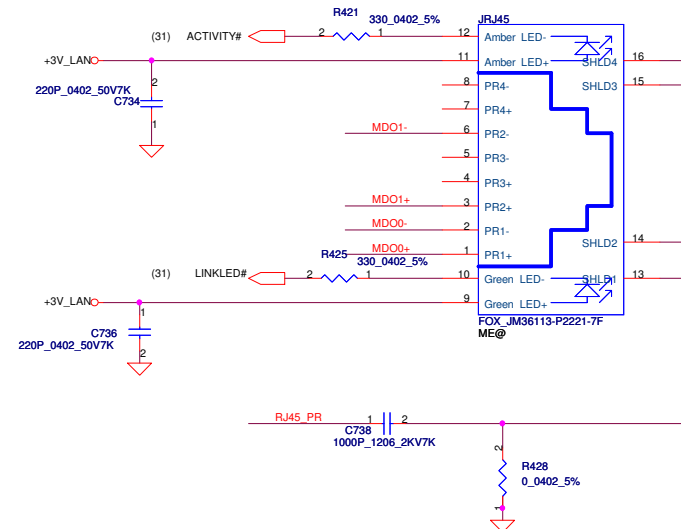
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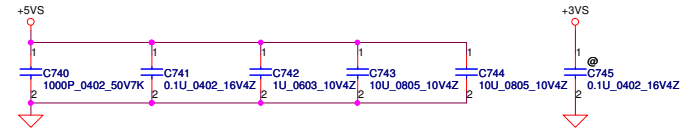
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



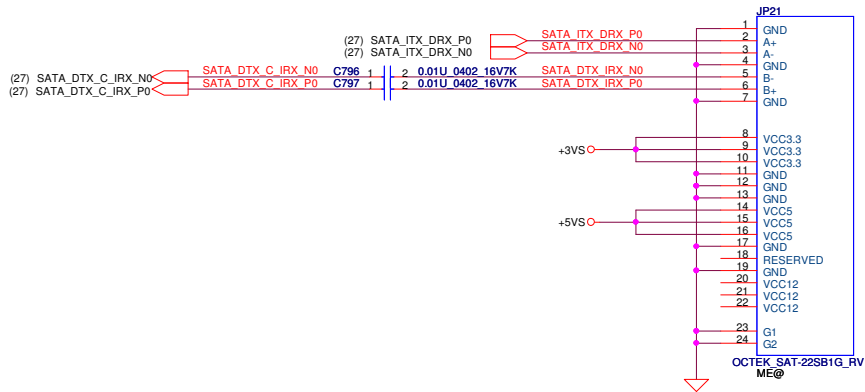
RJ45 CONN



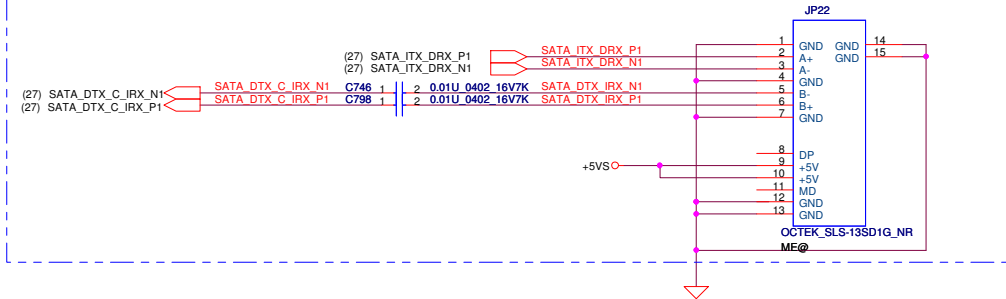
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2007/10/15				Title			
Deciphered Date				2008/10/15				LAN CONTROLLER			
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				Custom				Wednesday, March 18, 2009			
				Document Number				Rev			
				KIWA5/6 LA-5081P				0.4			
				Sheet				32 of 53			



SATA HDD Conn.



SATA ODD Conn.



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				B	KIWA5/6 LA-5081P	0.4
				Date:	Wednesday, March 18, 2009	Sheet 33 of 53

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF

CODEC POWER

(3.33V)
250mW

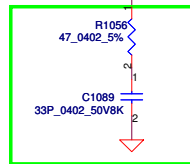
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

W=40Mil

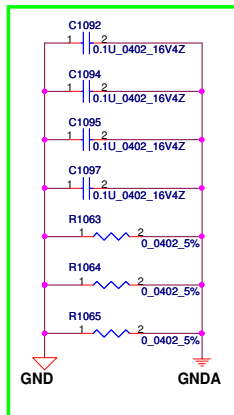
CX20548
AMOM DAA

11/20 update
PC_BEEP dB control



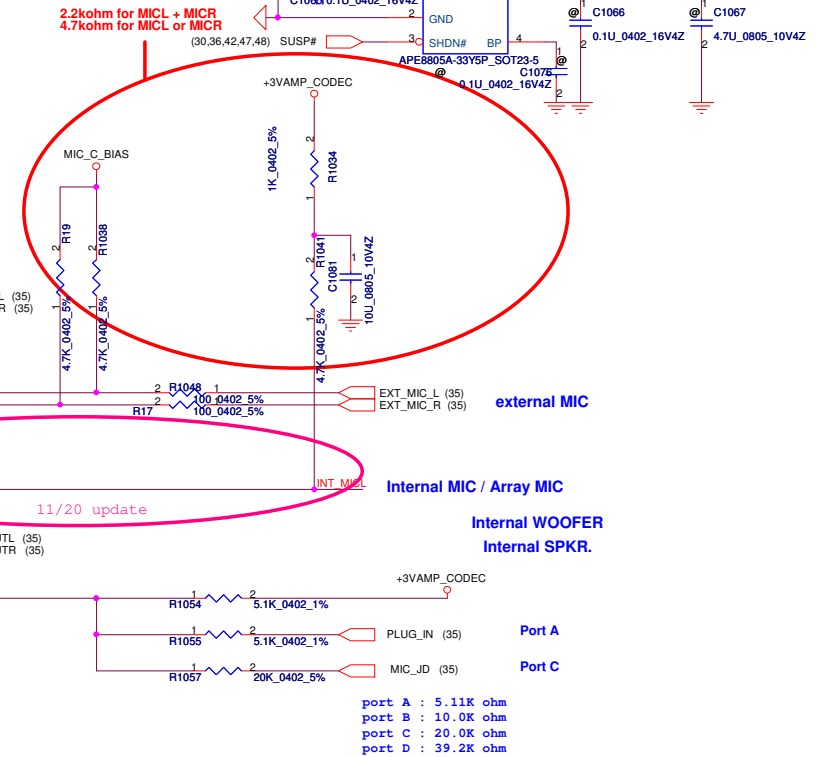
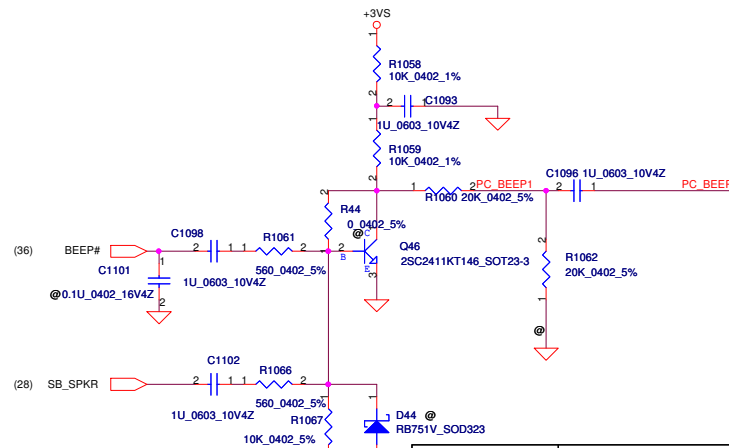
0216_Change value.

DIGITAL ANALOG



Place these C and R around AGND and DGND, then choose the one which is close to Codec to be accurate

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external MIC

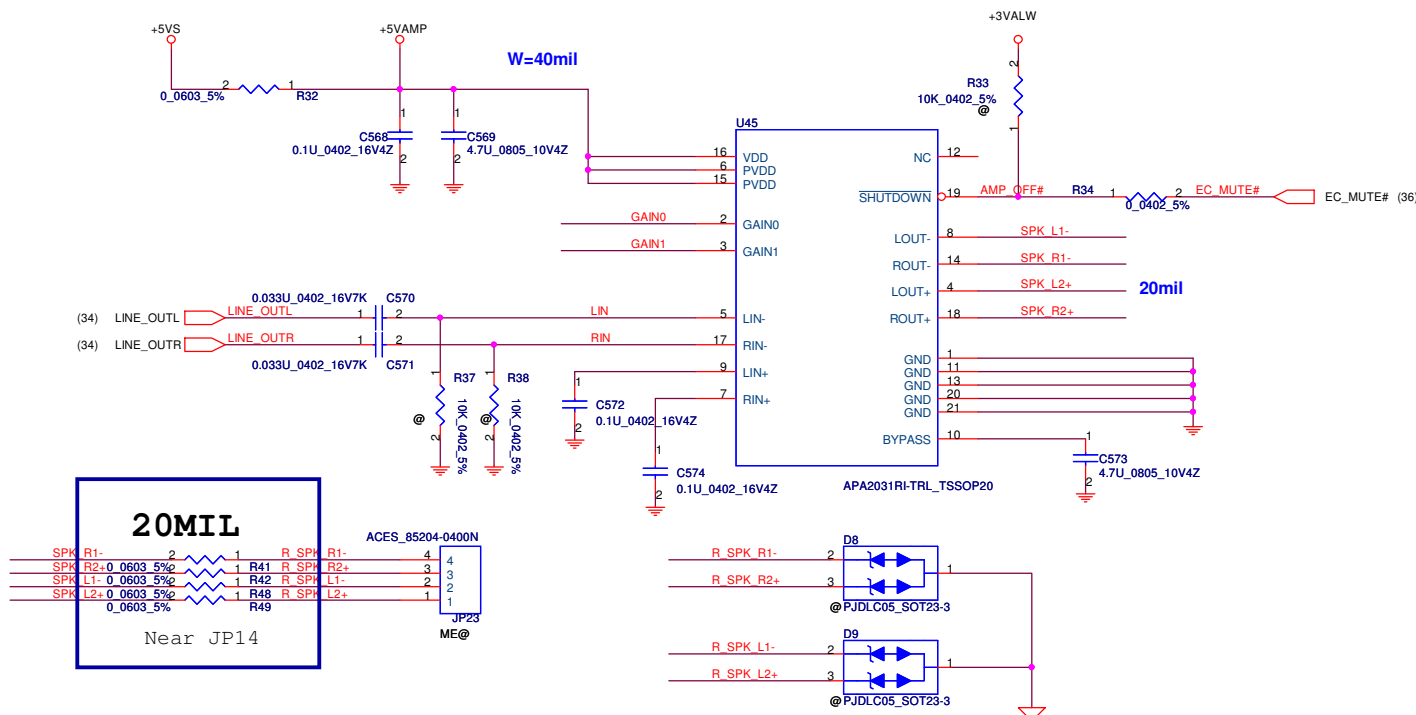
Internal MIC / Array MIC

Internal WOOFER
Internal SPKR.

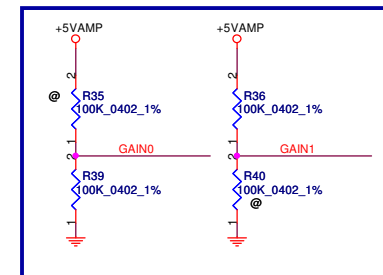
port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

Security Classification				Compal Secret Data		Title	
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				Custom	KIWA5/6 LA-5081P	0.4	
				Date	Wednesday, March 18, 2009	Sheet	34 of 53

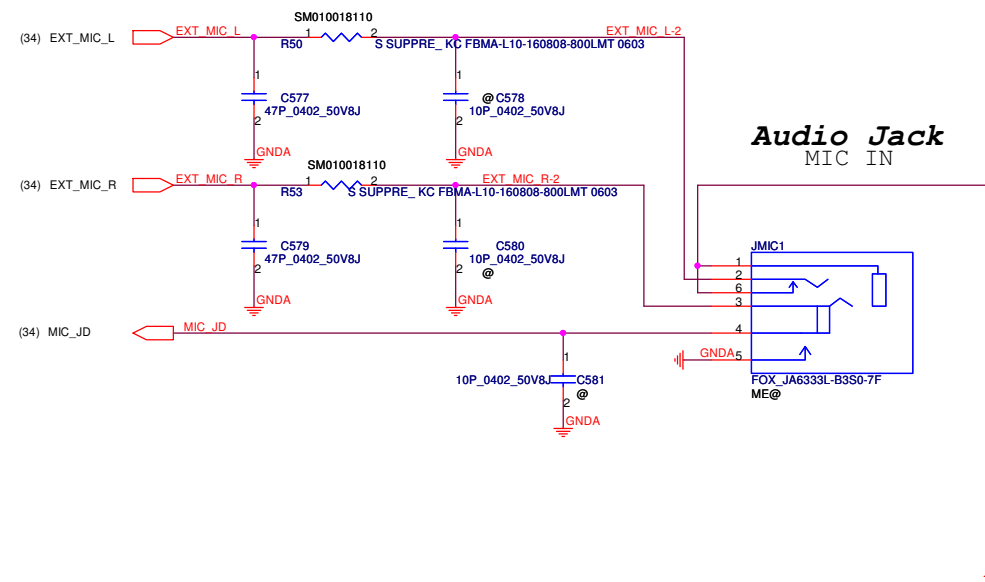
Speaker Connector



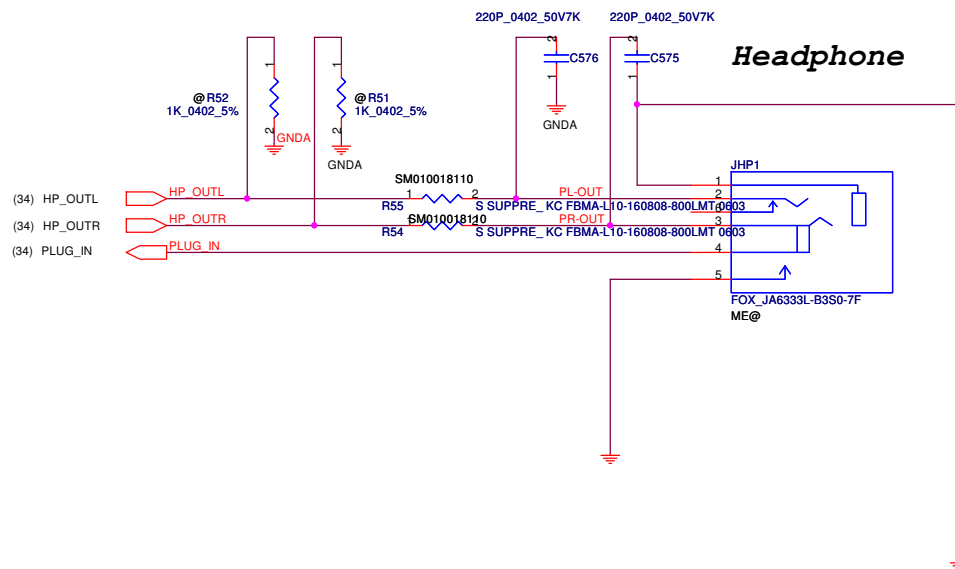
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



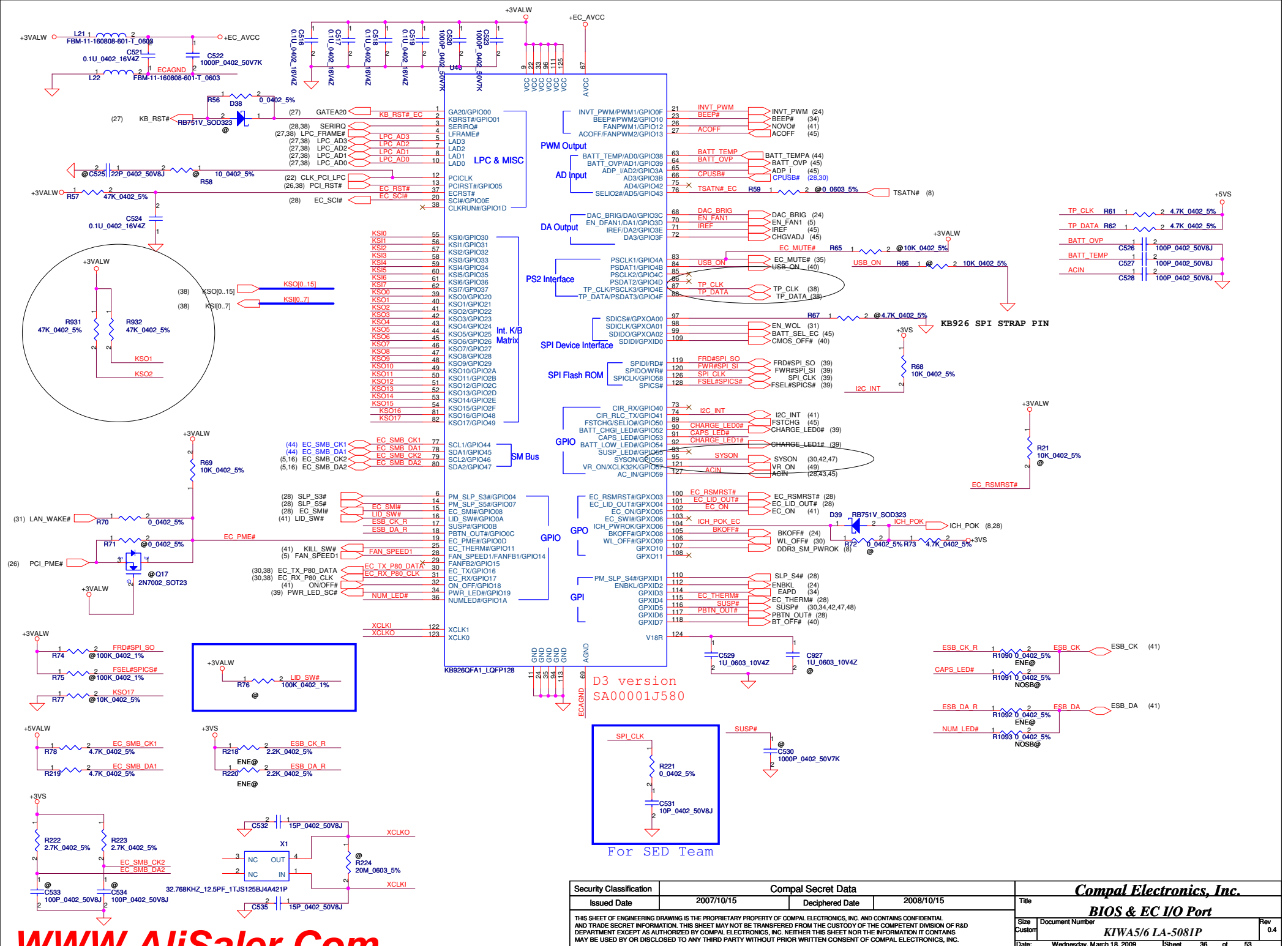
Audio Jack



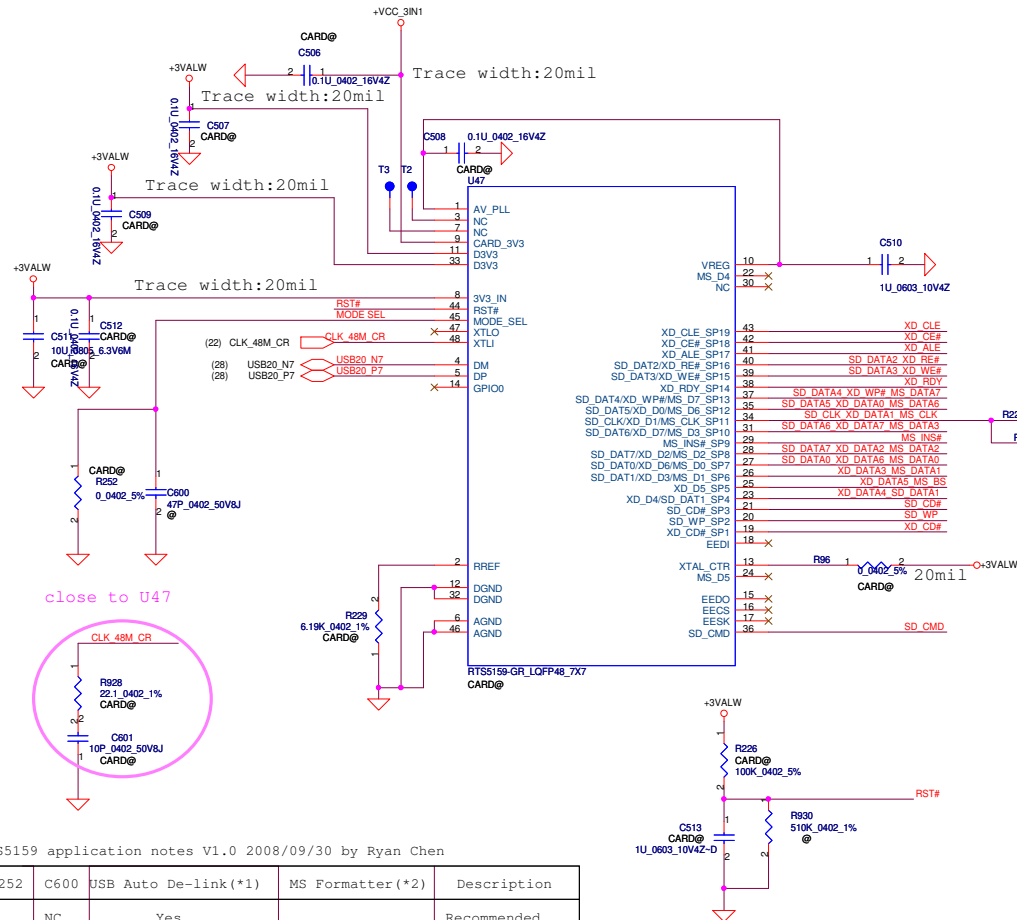
Headphone



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	AMP Audio speaker CONN
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				Document Number	KIWA5/6 LA-5081P
				Date	Wednesday, March 18, 2009
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				Rev	0.4



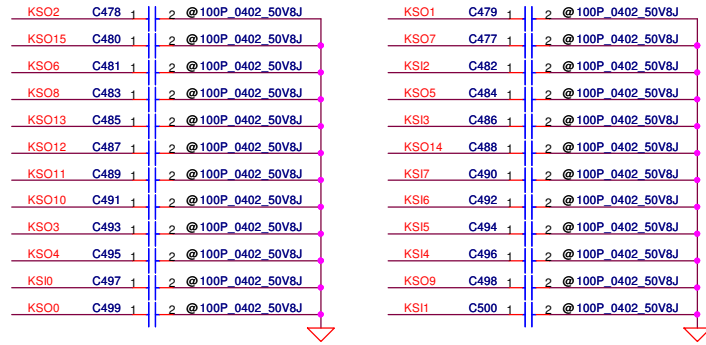
Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



Source:SP010001E00
2nd source:SP010001F00
30 pin

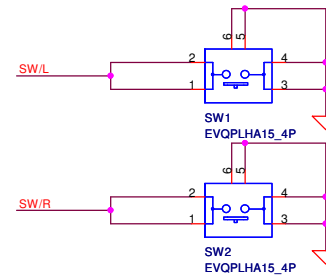
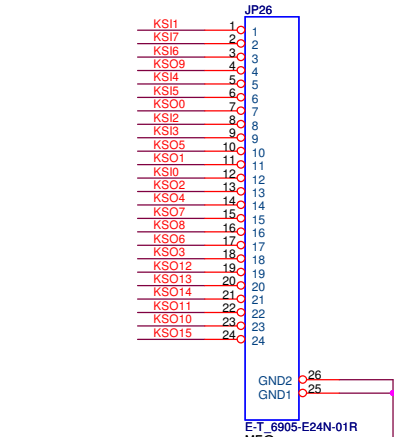
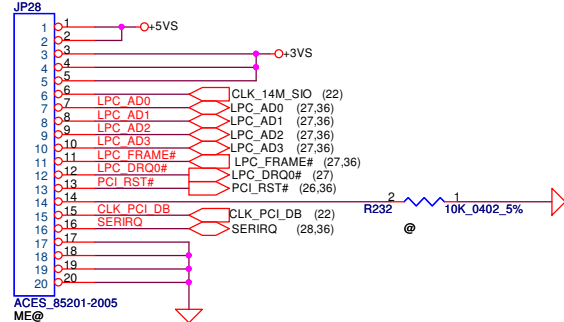
INT_KBD Conn.

KS[0..7] (36)
KSO[0..15] (36)

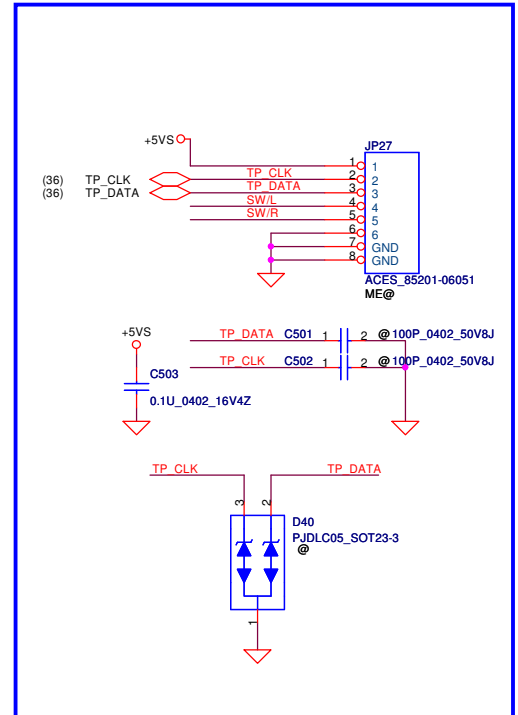
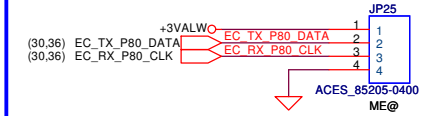


CONN PIN define need double check

FOR LPC SIO DEBUG PORT

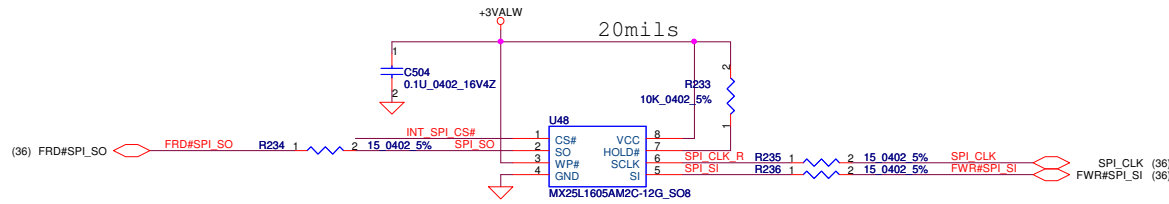


EC DEBUG PORT

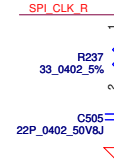
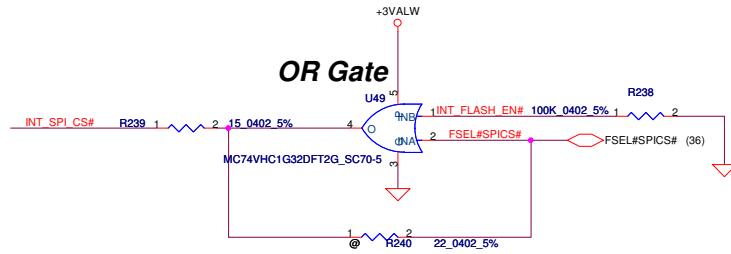


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				KIWA5/6 LA-5081P	
				Date:	Wednesday, March 18, 2009
				Sheet	38 of 53
				Rev	0.4

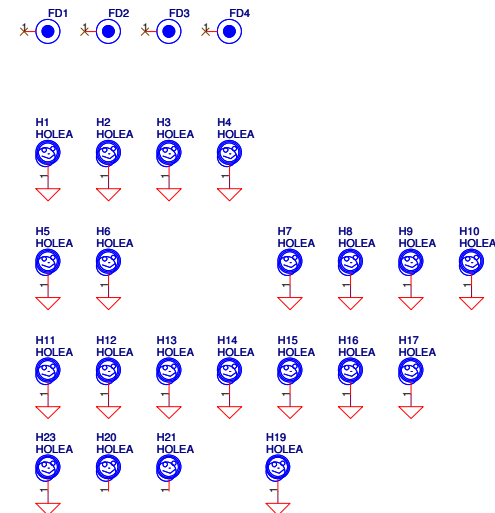
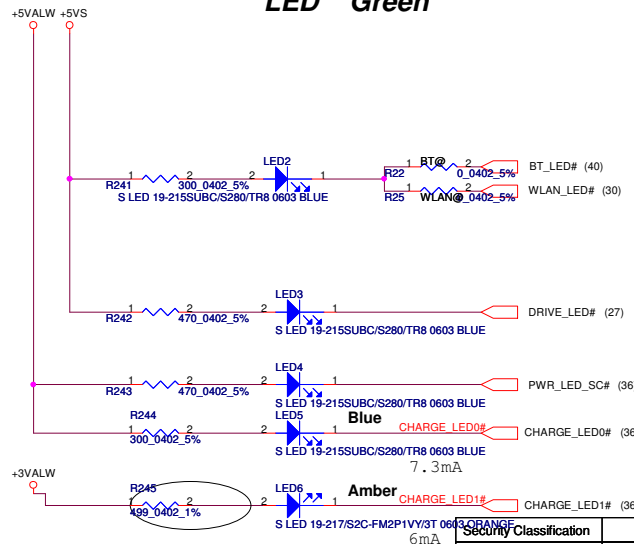
FOR EC 16M SPI ROM



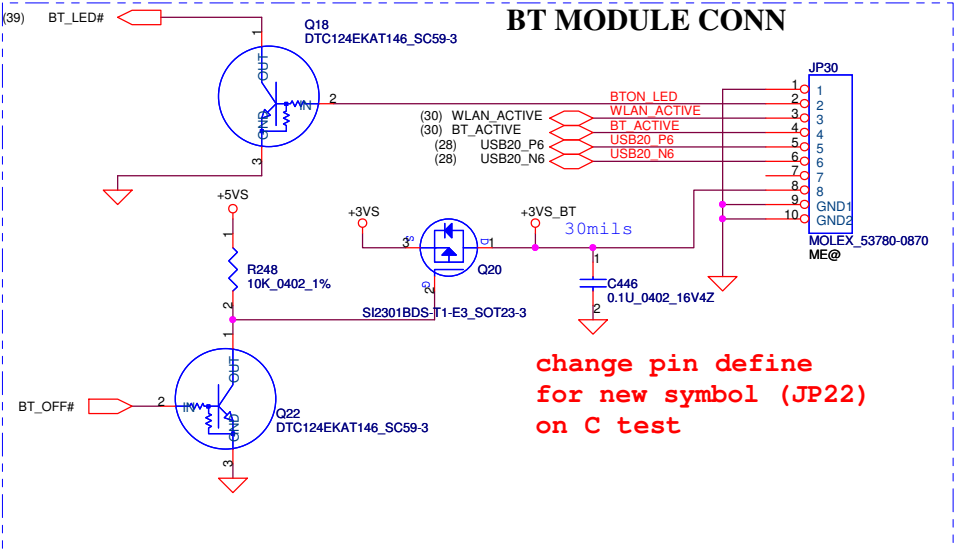
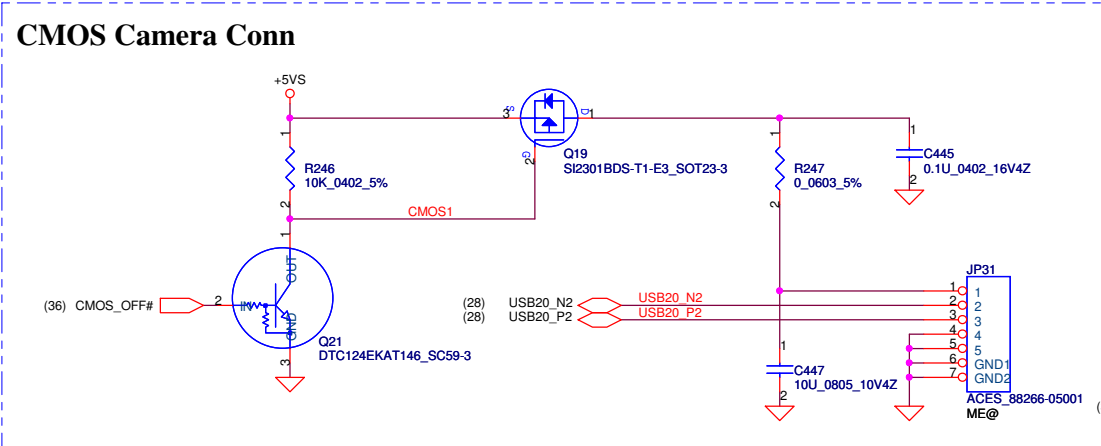
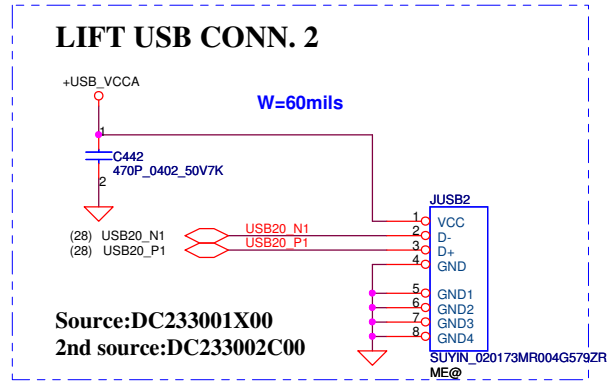
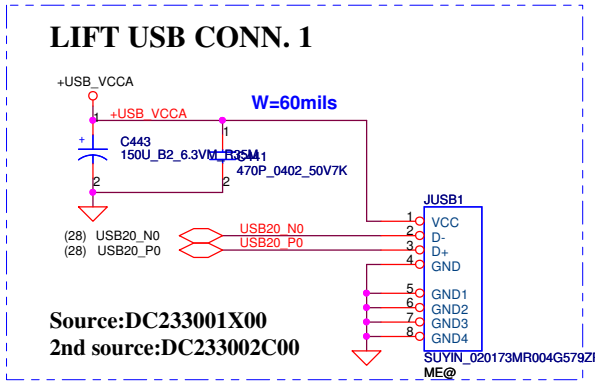
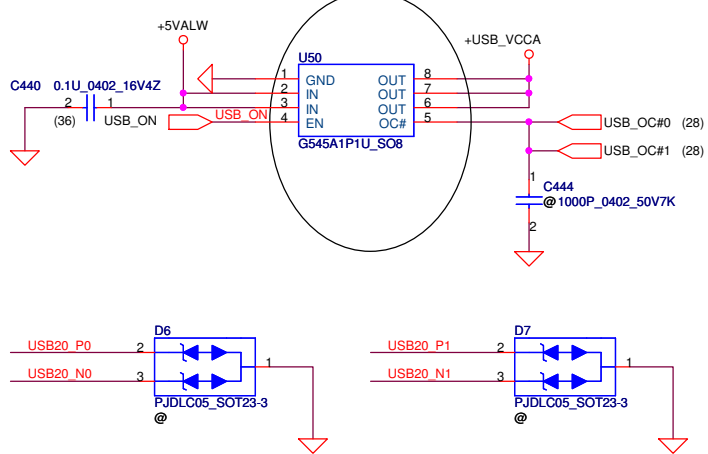
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



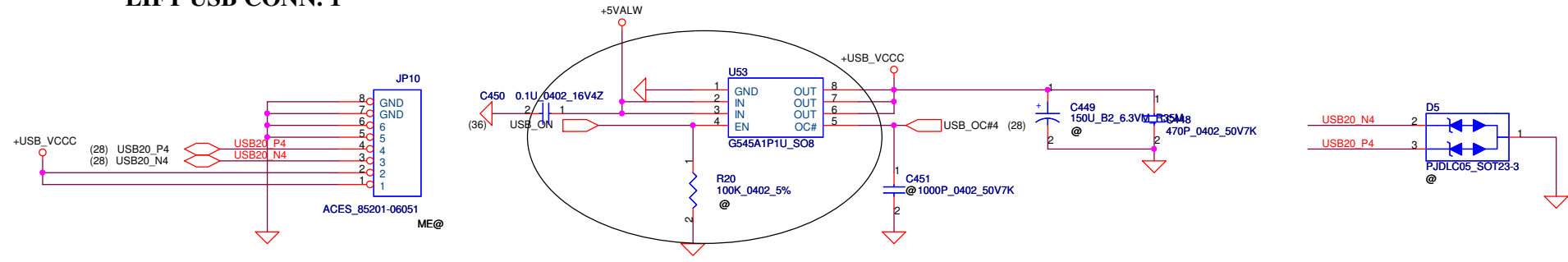
LED Green



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	LED/EC SPI ROM	
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					KIWA5/6 LA-5081P	0.4
				Date:	Wednesday, March 18, 2009	Sheet 39 of 53

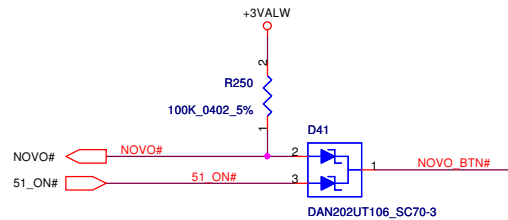


LIFT USB CONN. 1



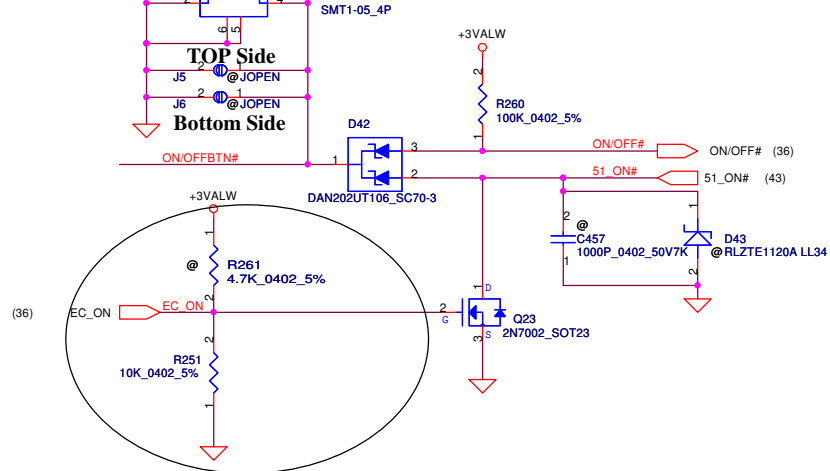
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Custom	Rev
				KIWA5/6 LA-5081P	
				Date:	Wednesday, March 18, 2009
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(36)
(43)

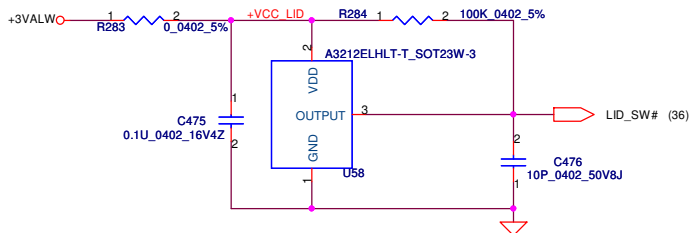


ON/OFF switch

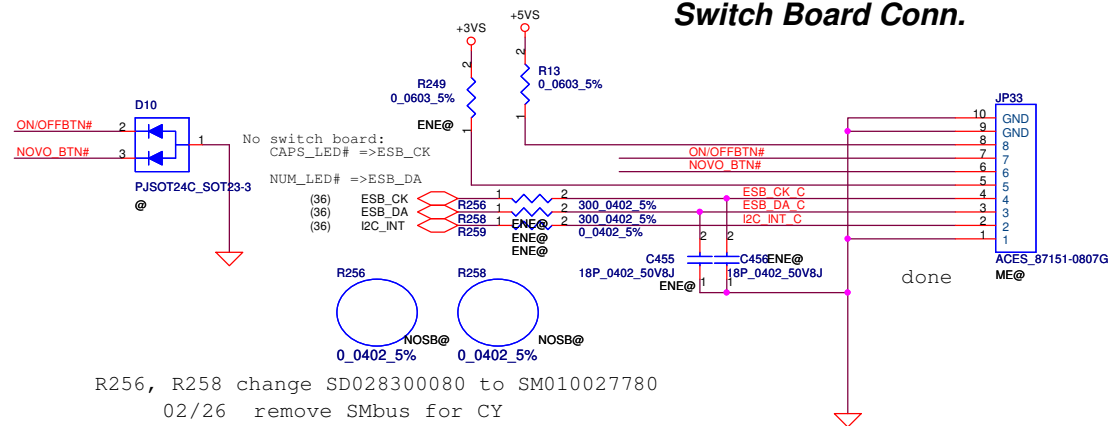
Power Button



Lid Switch

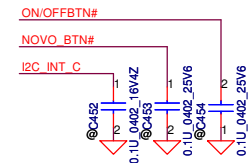
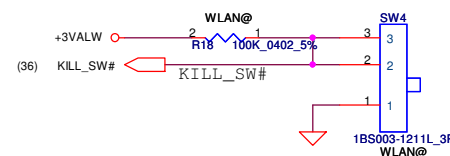


Switch Board Conn.

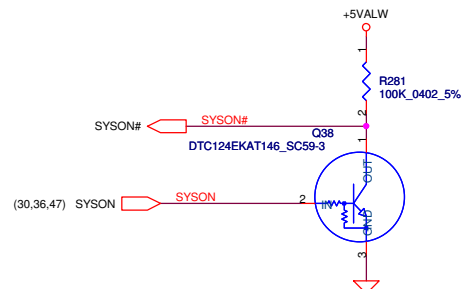
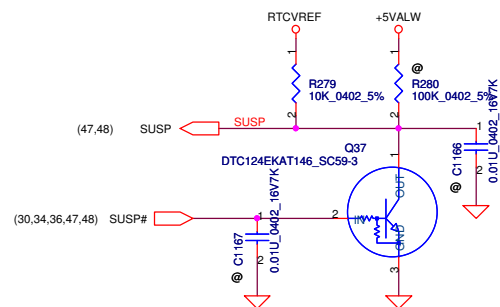
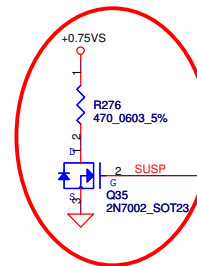
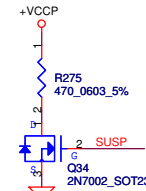
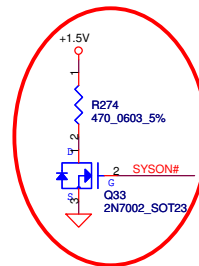
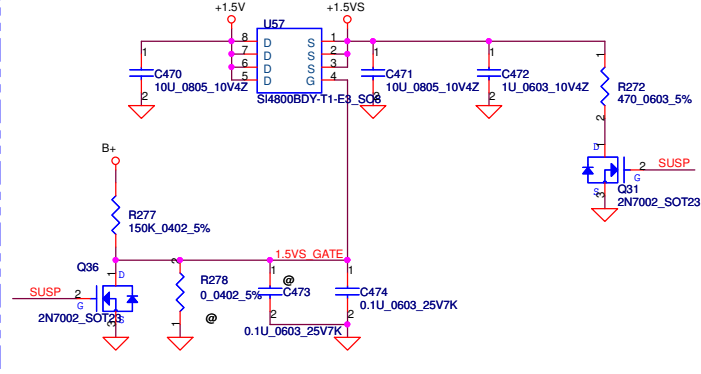
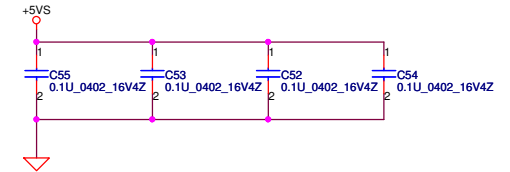
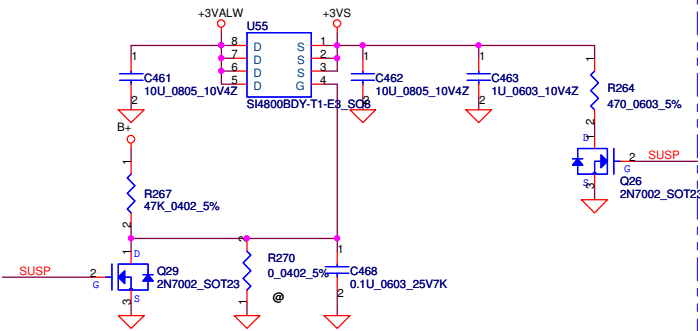
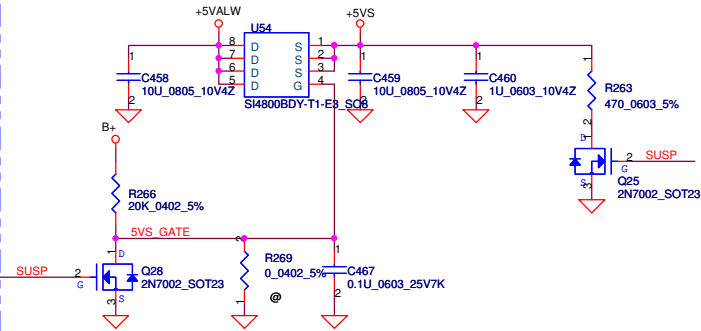


R256, R258 change SD028300080 to SM010027780
02/26 remove SMBus for CY

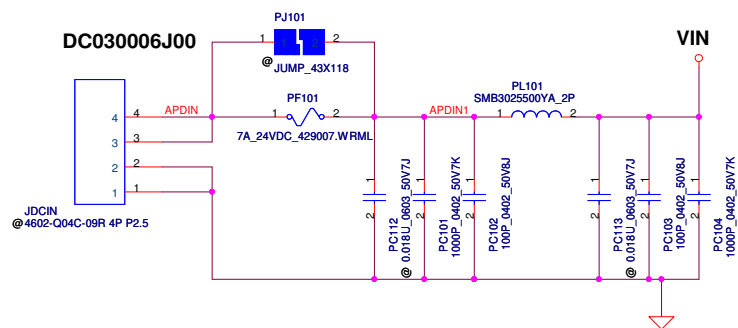
Kill Switch



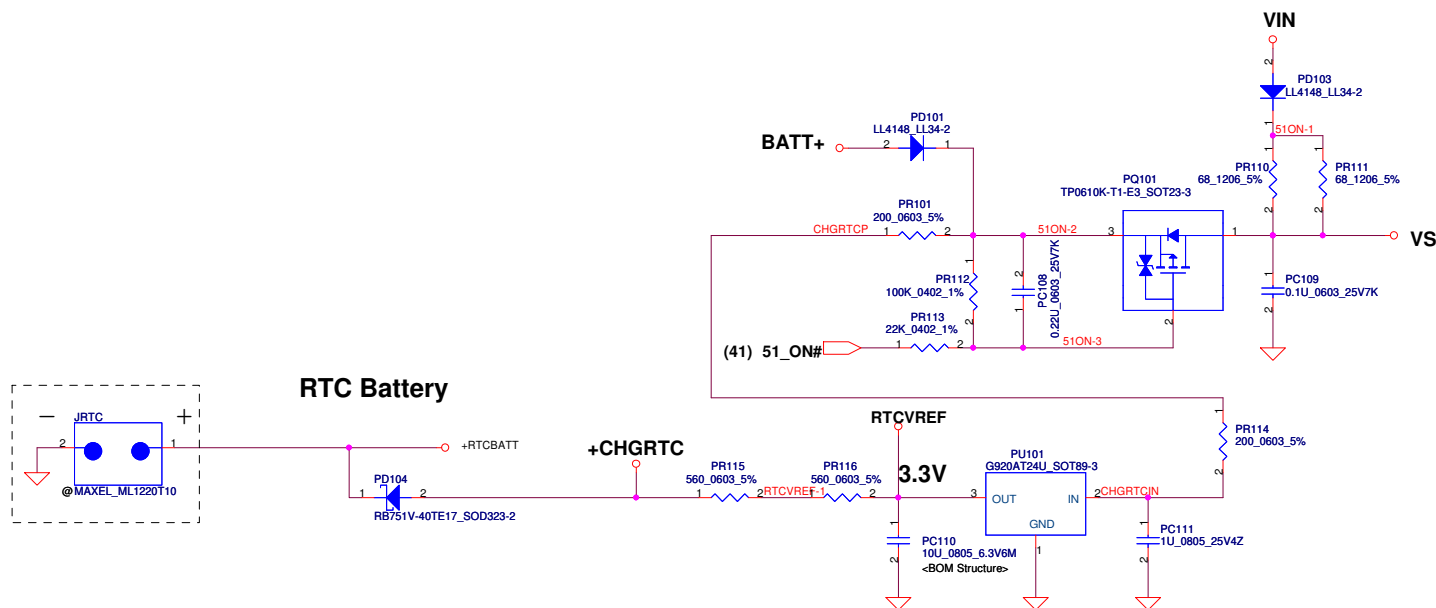
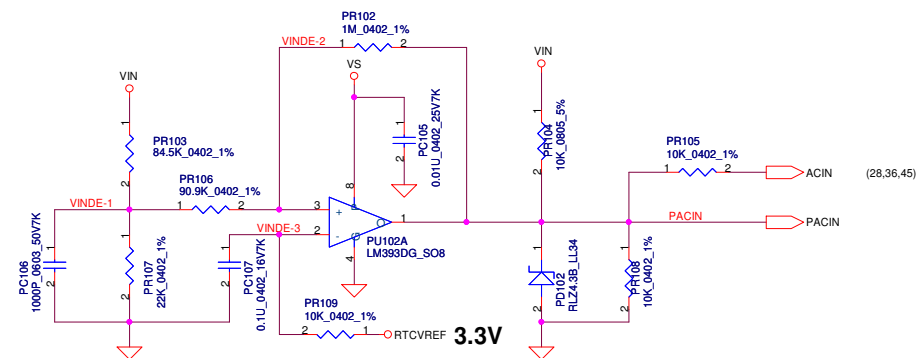
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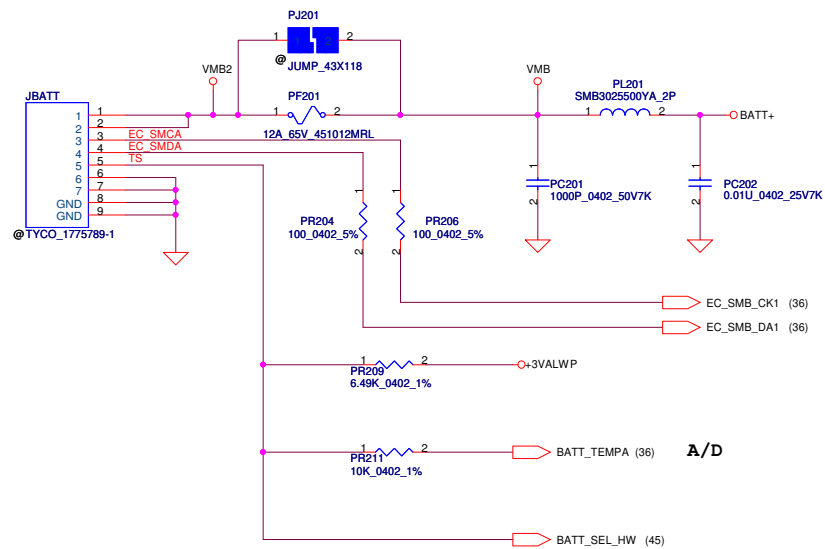
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title DC Interface		
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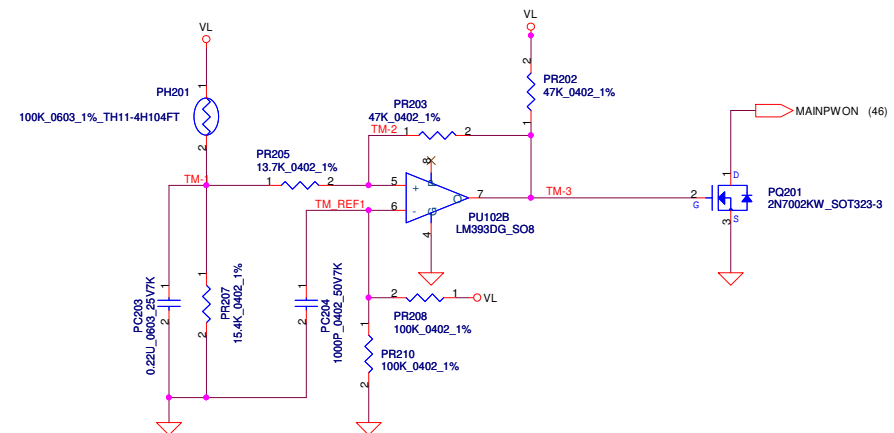
Vin Detector		
High	17.944	17.706
Low	16.242	16.027
	17.470	15.808



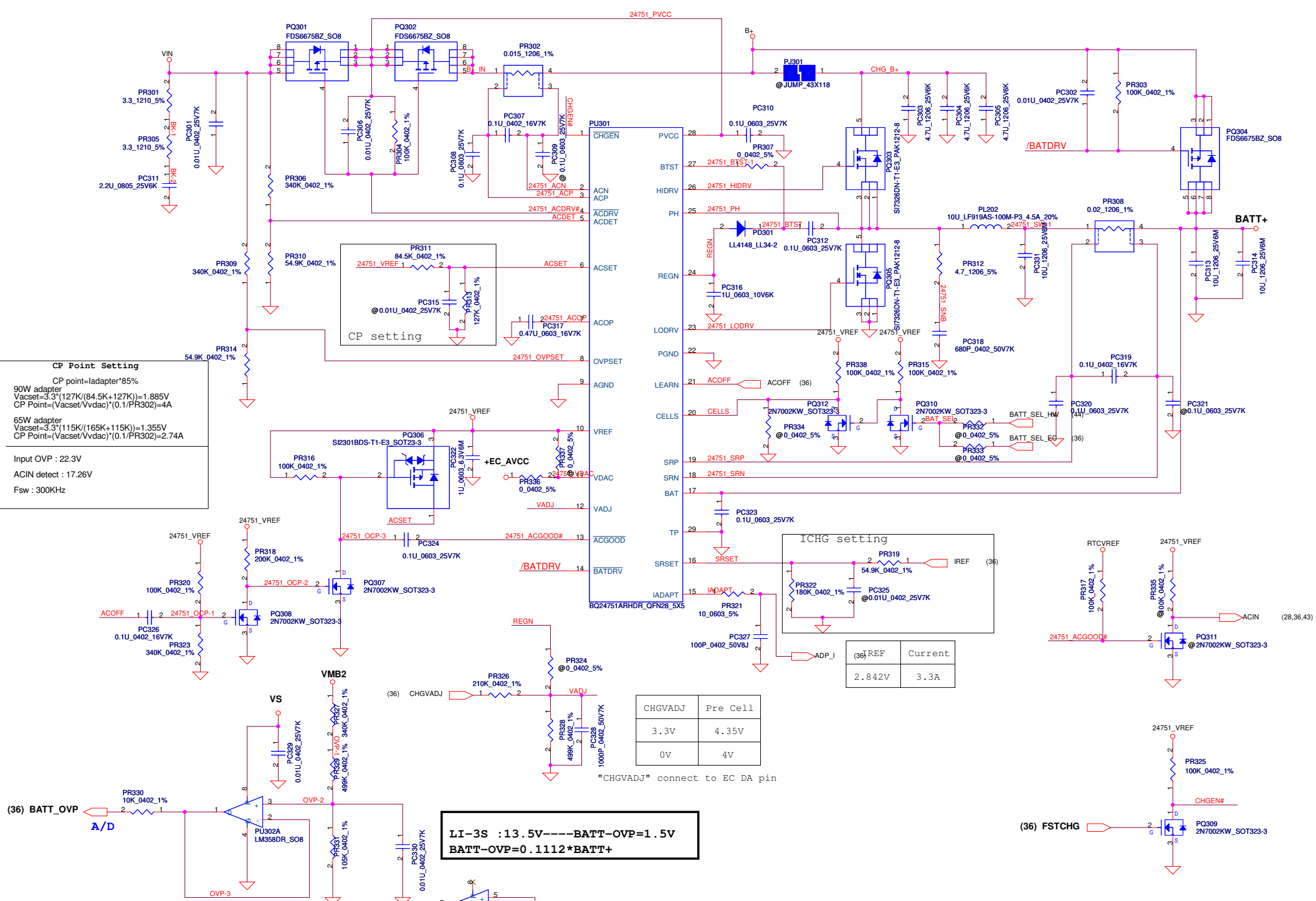
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								Size	Document Number	Rev
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



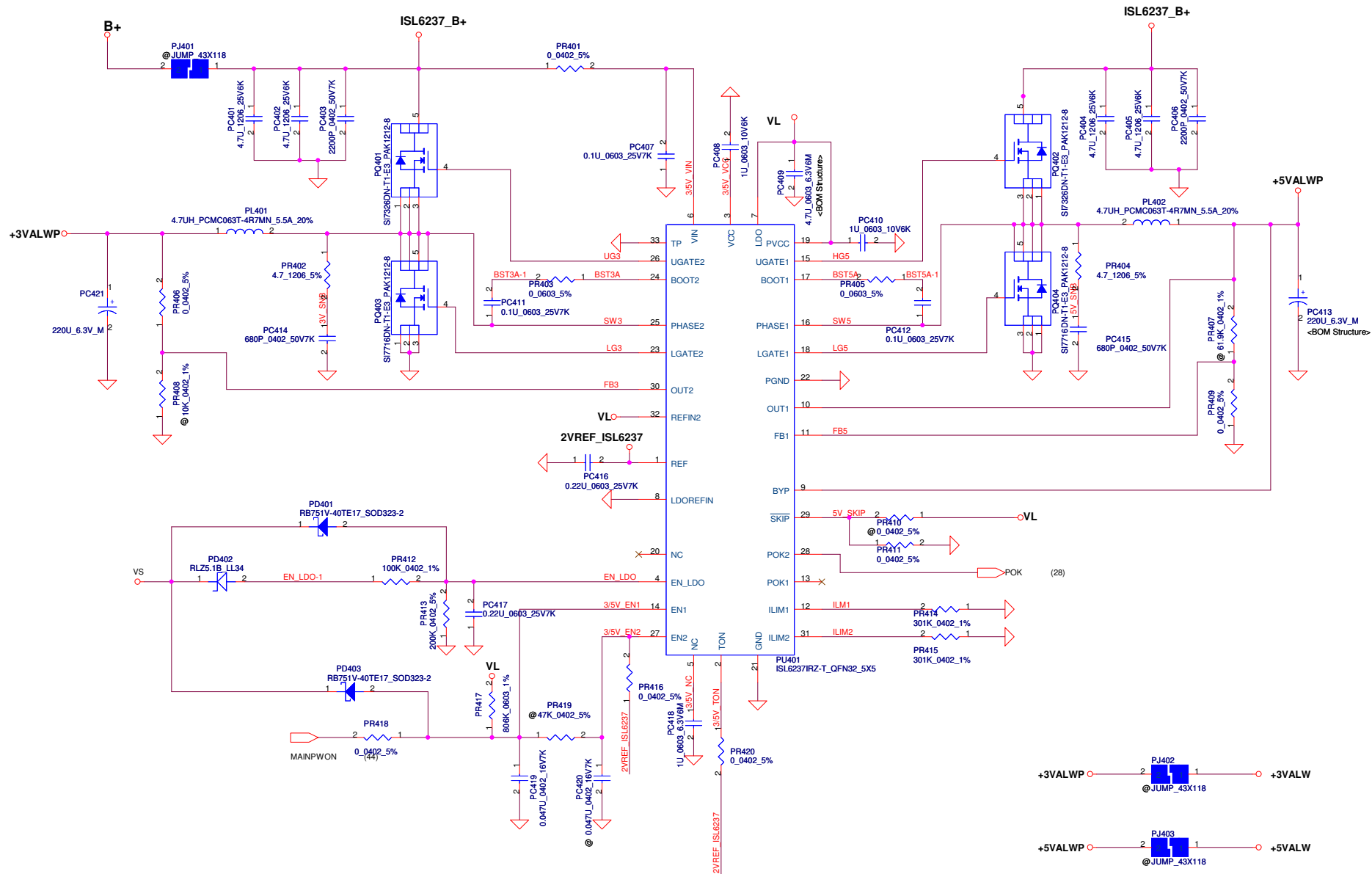
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Size	Document Number			Rev	
				0.4	
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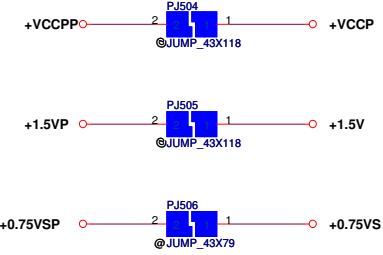
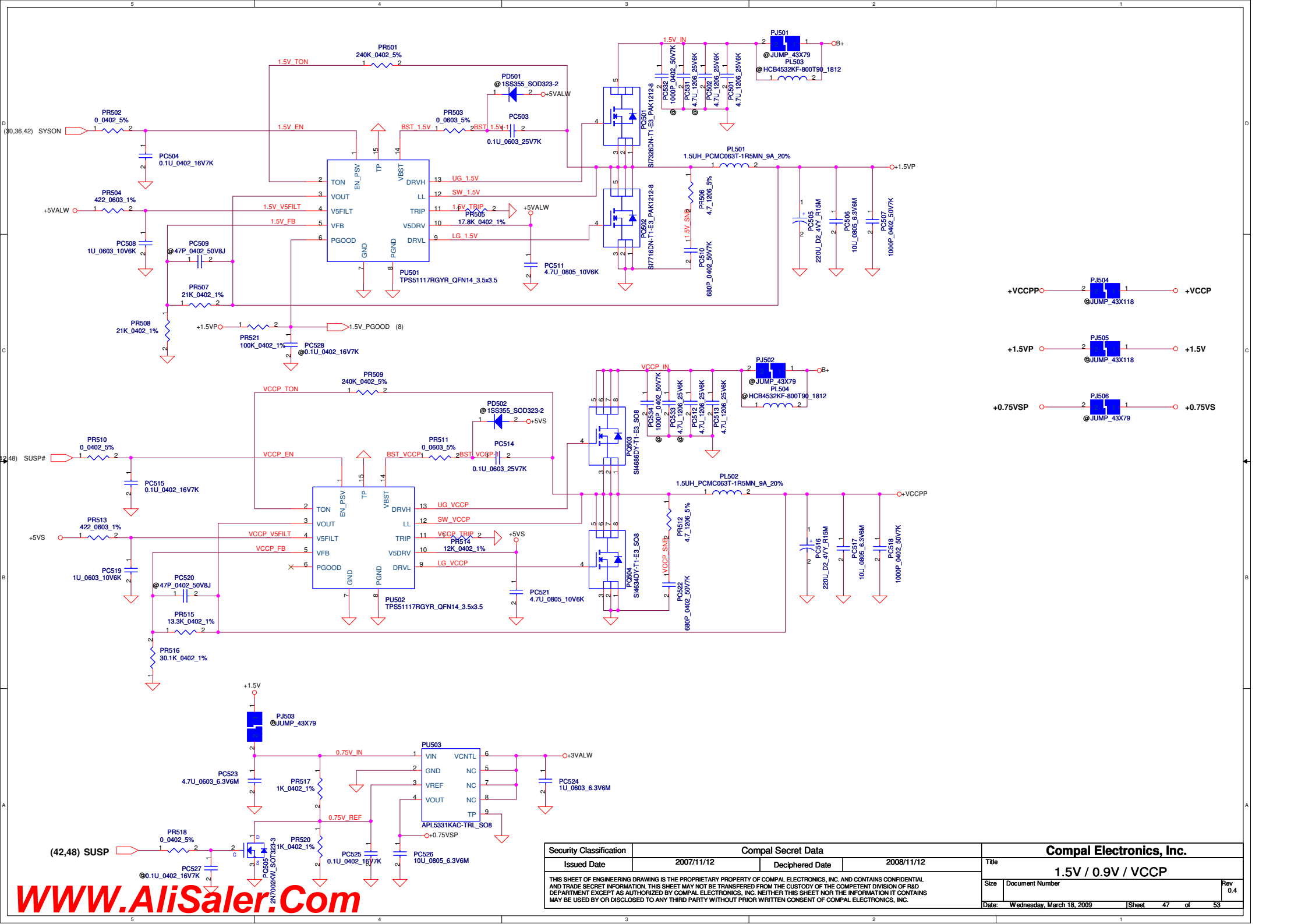
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

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Issued Date	2008/05/21	Deciphered Date	2009/05/21
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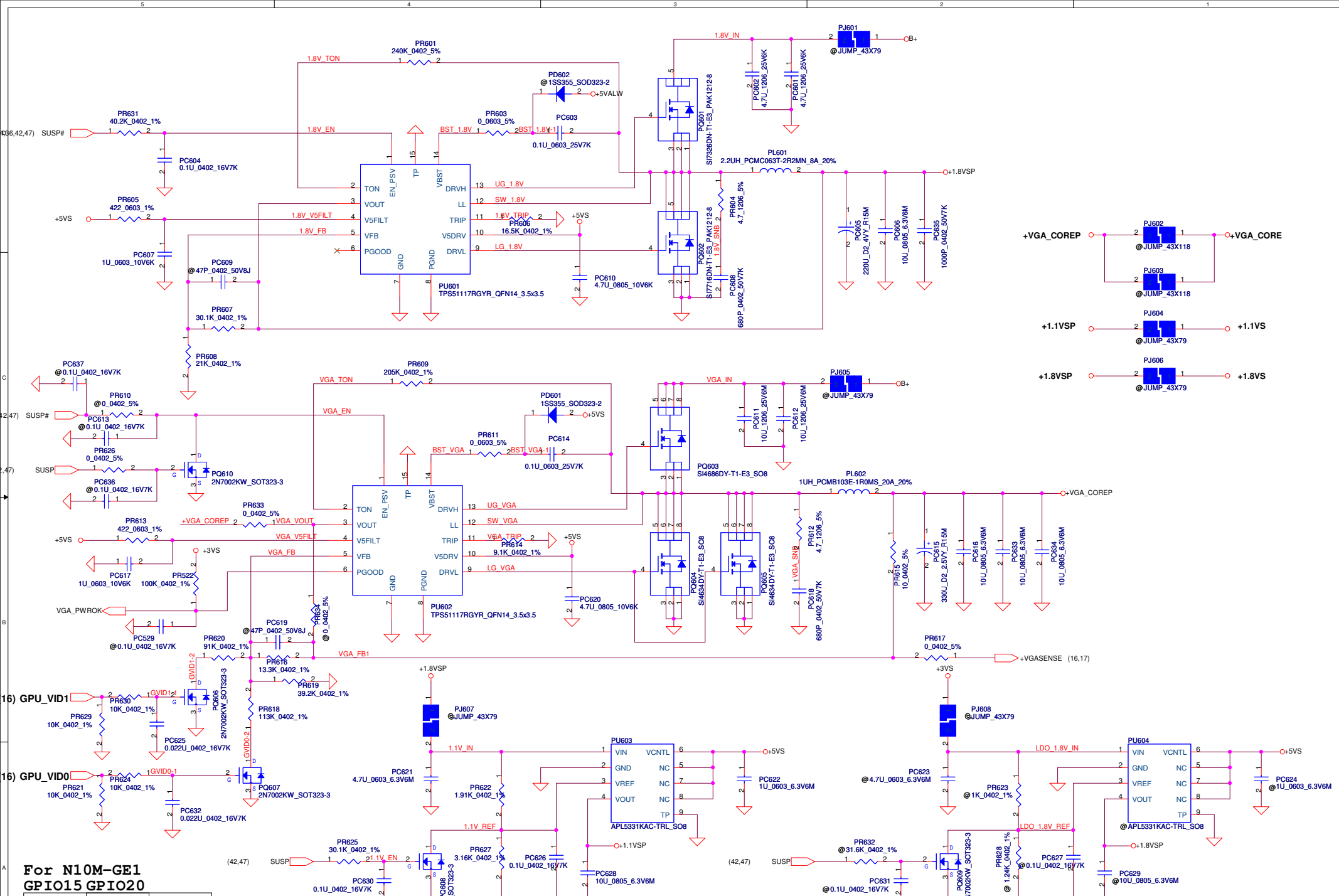
Compal Electronics, Inc.		
CHARGER		
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Date: Wednesday, March 18, 2009		Sheet 47 of 53		Rev	0.4

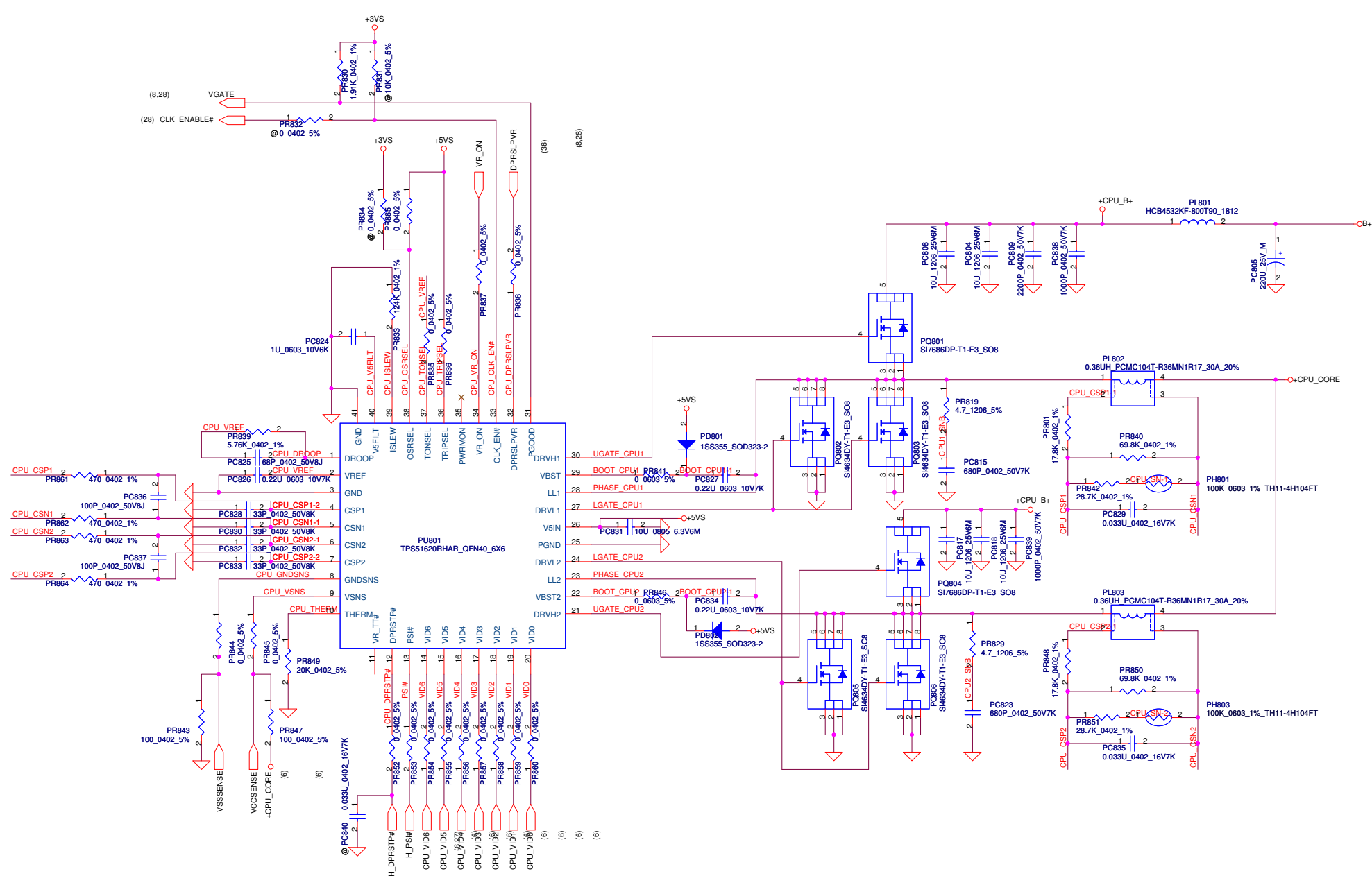


For N10M-GE1
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS
PR616=>9.09K
PR622=>2.21K
PR629, PR637, PC625, PC606, PR620=>un-pop
PR64, PR617, PC607, PR618=>un-pop

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2007/11/12	Deciphered Date	2008/11/12	Title
					VGA_CORE/1.8V/1.1V
Size		Document Number			Rev
					0.4
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				53	

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)		
3							
4							
5							
6							
8							
9							
10							
11							
12							
13							
14							
15							
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Size	Document Number	Date		Rev	
Custom	KIWAX LA-5082P	Wednesday, March 18, 2009		0.4	
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5			4			3			2			1		
NO DATE			PAGE			MODIFICATION LIST						PURPOSE		
1			12/10 39			Remove D11, and add R22, R25								
			12/10 36			change PWR_LED_SC# from U46.38 to U46.34								

